Proceedings of the 18th International Conference on System Theory, Control and Computing, Sinaia, Romania, October 17-19, 2014

Dual Priority Scheduling algorithm used in the nMPRA Microcontrollers

Subtitle as needed *(paper subtitle)*

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***Abstract*— In most of the safety-critical areas, including systems, avionics, automotive, and factory automation, the use of real-time time-trigger schedulers are encouraged due to their characteristics that does not allow interference to take place between safety-critical and non-critical components. Depending on the field where these types of schedulers are used, they can be categorized as preemptive or non-preemptive. In the automotive field, the non-preemptive schedulers are used where the system is safety relevant. The adoption of this strategy is used because offers a high predictability to the system, but can lead the system into failure. For this purpose it will be presented a solution where the switching of the context does not exist, therefore the use of critical sections is not needed any more. To achieve this performance we modified a static scheduler in a dynamic scheduler depending on the system status using Dual Priority scheduling and integrate the algorithm on a nMPRA processor. The new architecture provides a switching and response time for events within 5 to 8 machine cycles and guaranties that no task will suffer from starvation.**

Keywords*— *dual priority scheduling, real time system, nMPRA microcontroller

I. INTRODUCTION

Currently, the properties of a real time system depend, largely, on the scheduling algorithms used for the real time environment. The qualities of real-time scheduling algorithms have direct impact on the processing capacity of the system (number of tasks per unit time) and response time [1][2]. Using the fixed priority preemptive scheduling assure some benefits as a low runt-time overhead and the ability to support tight deadlines for high priority tasks [3]. The preemptive schedulers do not dominate non-preemptive schedulers in term of runtime overheads and amount of RAM memory consumption. In [3] the authors integrates both preemptive and non-preemptive schedulers which use the notion of preemption threshold [4], which was introduced by Express Analogic, Inc. to avoid unnecessary preemption. This new model, results in a dual priority system in which each task has a regular priority and a preemption thresholds which improves the schedulability of the tasks.

In [5] the proposed scheduling algorithm is Multiprocessor Dual Priority (MPDP), which splits priorities into three bands, upper, middle and lower. The hard task, that are considered period tasks, are assign two priorities, one for upper and one for lower band. The aperiodic tasks are considered as soft tasks and are assigned the priority of the middle band, which may be preempted by other hard tasks with higher priorities in the same band, by aperiodic tasks in the middle band or by any periodic task in the upper priority band. In this approach is guaranteed that the aperiodic tasks will have a reasonable answer in time, while the utilization of the system, is enhance.

The proposed model looks similar with our approach, with some differences:

- Our proposed Scheduler uses two different algorithms to schedule the tasks in order to have a functioning system no matter how is the load of the tasks from the system.
- The scheduler uses three different priority tasks to use two different scheduling algorithms.

II. THE NMPRA ARHITECTURE

The first version of nMPRA has been defined in [6] and [7]. In [8] the nMPRA architecture has been improved for the scheduling process. To the current nMPRA architecture was added a slow bus with a Buss Controller and a peripheral in which the scheduling algorithm was embedded (Fig. 1). The scheduling algorithm was removed from the nHSE block and embedded into a peripheral because the hardware tasks will be configured with the help of its internal registers. At this moment the processor architecture have been transformed into microcontroller architecture.

This new approach optimizes the switching of the hardware tasks in terms of silicon costs and system complexity. During this process we encounter some synchronization issue, caused by the current architecture of the processor, MIPS with 5 pipeline stages. In order to stop a working task the Program Counter (PC) must be stopped. The switch process of a task is really simple and is done in two steps.

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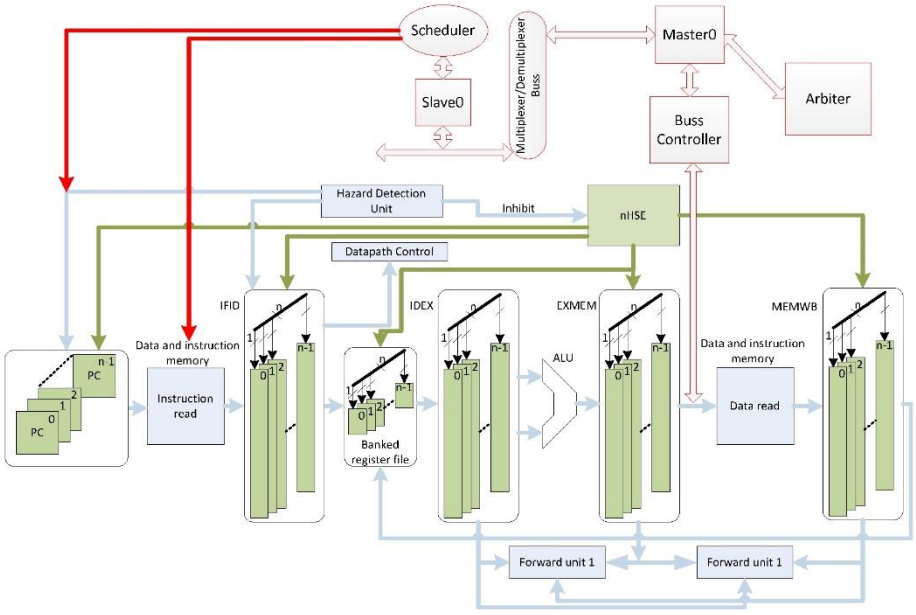

Fig. 1. The nMPRA architecture (source [8])

- Stop the PC of current task.
- Select the appropriate task to share the resources.

From this description we can think that the switching of a task can be done in 1 machine cycle, because the stopping of the PC and the selection of the appropriate input/output of the multiplexer/demultiplexer can be done simultaneously.

It could be true if there were no decencies with the RAM and ALU that are shared. So when the *SelectTask[2..0]* bus (Fig. 2) will have a different value, in order to select the new task, the ROM, ALU and ALU will no longer be available for the current task.

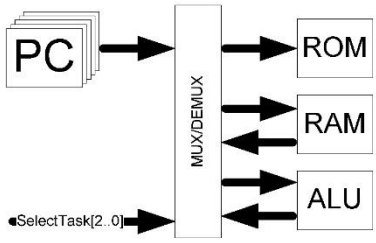

Fig. 2. Simplified nMPRA architecture

We've choose to wait 3 machine cycles to solve the synchronization issue. The other 2 machine cycles are used to synchronize the next task program counter address with the ROM memory and the instruction fetch pipeline register because the Scheduler and the program counter are using 3 quadrature clock signals.

III. The Proposed Dual Priority Algorithm

In this paper we are treating the dynamic scheduling. In the [9] the switching time was between 1 and 3 machine cycles while in this paper the overall switching time of a task is 5 machine cycles because the RAM, ALU and ROM are shared between multiple resources (Fig. 2) using only one big multiplexer/demultiplexer. In order to have a better understanding of the algorithm we are going to reuse and detail some of the information from [9].

In the following lines, the classes that each task can belong are presented:

- The class of active tasks, which has the higher priority (the tasks will be inserted only in the active task queue (ATQ)): will schedule the tasks, based on priorities, only in the Running State (RS) of the Scheduler.
- The class of interrupted tasks, which has the second priority (the tasks will be inserted only in the interrupted task queue (ITQ)): will schedule the tasks, based on priorities, only in the Idle State (IS) of the Scheduler.
- The long execution tasks class (significantly exceed the base period T corresponding to the priority task), which as the least priorities (the tasks will be inserted

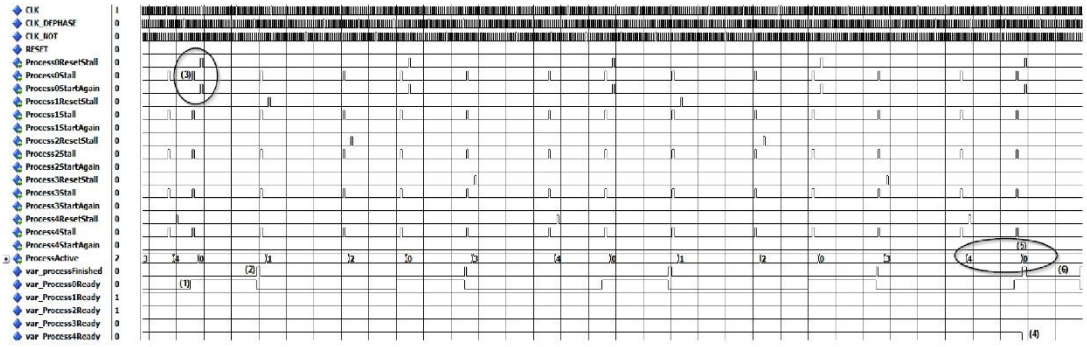

Fig. 3. Overall view of the task switching system

only in the long task queue (LTQ)): will schedule the tasks, based on ROUND ROBIN (RR) algorithm, only in the Idle State (IS) of the Scheduler.

Emerged into the Scheduler, a global Round Robin timer (TRB) exists that is used to supervise the active time of the current task and also used as a task occurrence for the long tasks.

Knowing that the timer is used to measure the active time of a task and stop it if it takes too long to execute, we will have to be careful with the time values that are going to be used for the tasks supervision. In order to have a functional scheduler, the TRB should be initialize with the occurrence of the slowest task from the system or less. However, this configuration depends on the system architect.

In Fig. 4 is presented the operational flowchart of the Scheduler (event driven), which is driven by the main clock signal of the processor. The events can be generated by the expiration of the TRB and the activation of the tasks.

In order to illustrate the algorithm better we are going to assume that processor executes 5 tasks with 5 different priorities.

At some point one task became active, the TRB will start to decrement and the Scheduler will enter the RS. If the task, for some reason, takes more time than usual, the TRB will expire and the current task will be inserted into the long task queue. But if the task is going to finish its execution before TRB expires, the Scheduler will enter IS.

Assume that another task became active, starts to execute code and another task, with greater priority, became active. The first task will be interrupted and inserted into the ITQ and the task with greater priority will take its place. After active task finish its execution, the Scheduler will leave the RS and enter IS and the interrupted task will resume its execution. For a better illustration of this example we assume that all the 5 tasks became active, in the end one task will run and the other 4 will be inserted into the ITQ. After the current task finish its execution and the Scheduler leave RS and enter IS the 4 task will be scheduled based on priority.

Now let's take another example. All of the tasks are slow and will be inserted into the LTQ. After the Scheduler will leave RS and enter IS, the priorities of the current tasks will not matter, because the long tasks will be scheduled based on RR algorithm. The amount of time that each task will have is equal with the time from TRB. When a task finishes its execution, during this state, it will be inserted into the ATQ and removed from LTQ.

Because of this TRB and the RR algorithm the system cannot be blocked by any task.

In Fig. 3 are presented 5 tasks that are scheduled by the algorithm. In the following lines there will be a description regarding the relevant signals, from the point of view, that are used in switching process:

a) clk, clk_dephase,clk_not – are the clock signals for different modules from microcontroller.

b) processXstall (X will have values from 0 to 4) : force the current task to enter low power mode. In this state the task will not execute any instructions.

c) processXresetstall (X will have values from 0 to 4): wake up the current task that is in low power consumption.

d) processXstartagain (X will have values from 0 to 4): select the active address, with the help of the program counter, of the task that is going to be released.

e) Processactive[2:0]: represents the number of the active task.

f) var_processXready (X will have values from 0 to 4): represents the event when a task became active. That does not mean that it will start to run. The signal will be high as long as the task is executing code or is active and in low power mode or just interrupted.

g) var_processfinished: task finishes execution.

In Fig. 3 can be seen that the Task0, which has the highest priority, is scheduled periodically ((1) from Fig. 3). The var_process0ready signal will be high as long as the task is executing code. The var_processfinished signal ((2) from Fig. 3) shows that the Task0 finish its execution successfully and enter low power mode ((3) from Fig. 3).

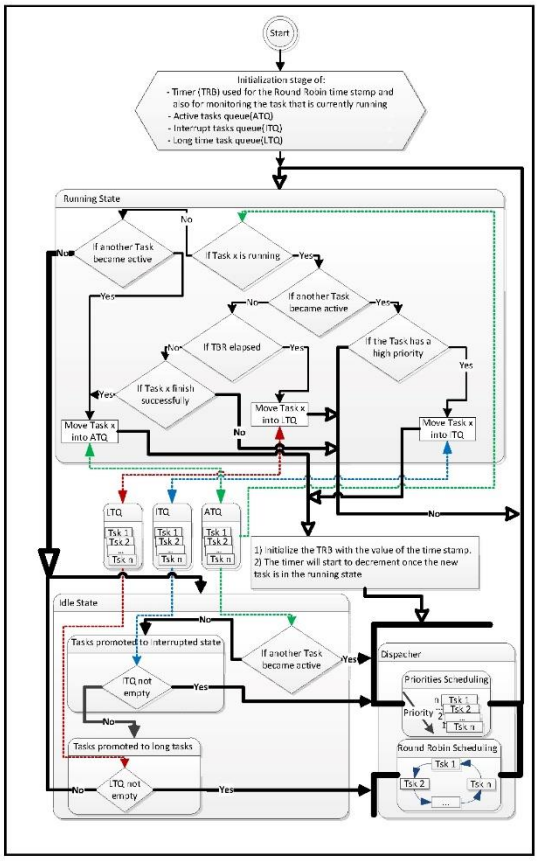

Fig. 4. The flowchart of a scheduler with a dual priority algorithm proposed (Figure 3 from [9]).

In (5) from Fig. 3 a task switch take place. Task4 finish its execution successfully ((4) and (6) from Fig. 3) and Task0 will start to execute code.

If the TRB and the occurrence of the tasks are not chosen properly, the following situation can occur:

- Priority inversion: There are 3 tasks with different priorities. The task, with intermediary priority, is running and is interrupted by the second task with higher priority. The task that was interrupted is now in the ITQ and the current task finishes its execution, but at the same time, the third task, with lower priority became active. In this particularly case the task from ITQ will not run, even though it has higher priority, because the new task is located into the ATQ
- Task starvation: Assume that we have 10 tasks with different and same priorities. If one task is interrupted by another task, with higher priority, this task will be introduced into the ITQ. From this point forward all of the tasks are going to succeed properly forcing the Scheduler to remain in the RS. Because the ITQ and LTQ are used only in the IS, this task will starve. If another task is interrupted, it will be inserted into the ITQ. At this moment the balanced is broken because the Scheduler will have time to enter the IS and one of the two task will be inserted again into the ATQ based on priority.

The particularly cases that were mention above can be avoided by choosing the right occurrence for each task in order to let the Scheduler enter IS. Let's assume that we enter in one of the particularly cases described abode because the frequency chosen for the processor is too small for the complexity of the whole system. The situation can occur quite easily because the project manager did not foresee that the functionality of the entire project can be increased considerably at the demand of the customer.
In this case the system can be configured to work only in a Round Robin manner, each task will have the same occurrence. The configuration of the whole system will not be affected at all by this approach because the only thing the programmer has to do is to insert the code from each task into an infinite loop. Because of this infinite loop the task will never end and each task will be promoted to LTQ.

IV. Results

The first steps, which were taken to obtain the current microcontroller architecture was an approach from simple to complex.

The first and the most important step was the designing of a simple, but functional MIPS processor. After a proper testing, the processor architecture was improved with more than 35 instructions, ultimately leading to a number of 42 instructions. The next steps, that were more complex, were to modify the current processor architecture to support 5 hardware threads. In order to achieve these results the following resources were added:

a) A big multiplexer/demultiplexer: used to select the active task.

b) A slow bus: that is clocked at the microcontroller clock line.

c) The dual priority scheduler: used to switch tasks.

The whole architecture was design using VHDL hardware description language (VHDL 93). Altium Designer 2014 was used, only as a text editor, to include the individual VHDL module and create the architecture. The design created was simulated using ModelSim Altera Started Edition 10.1d. The only stimulus applied to the microcontroller was the 3 quadrature clock signals because the ROM memory was already initialized with the machine code for all 5 tasks.

The following results were observed, in normal operation, at key points. In the following lines we are going to detail the steps required to do a task switch:

a) var_process0ready ((1) from Fig. 5)) signal represents the event occurring after activation of the first task. Because no jump instruction is performed all of the active task will be stopped with the help of processXstall (X will have values from 0 to 4) signal. The process1ready will remain active as a sign that the task is still active. At this moment task1 will be in the ITQ.

b) Wait one clock cycle.

c) Processactiv signal selects thread 0 as the active one (3) from Fig. 5).

d) Process0resetstall and *process0startagain* signals are activated ((4) from Fig. 5).

As we can see from Fig. 5 the response time of the scheduler is one machine cycle (between (2) and (5)), the time spent after the task with higher priority became active and the starting of executing code (between (2) and (5) from Fig. 5) is done in 5 machine cycles in an interval of 75ns, where the period of the clock is 15 ns.

V. CONCLUSIONS

The current paper presented, in a more detailed manner, the dynamic dual priority algorithm presented briefly in the [9]. The main idea of the dual priority algorithm was to keep a functional operating system no matter how difficult were the requirements of the system.

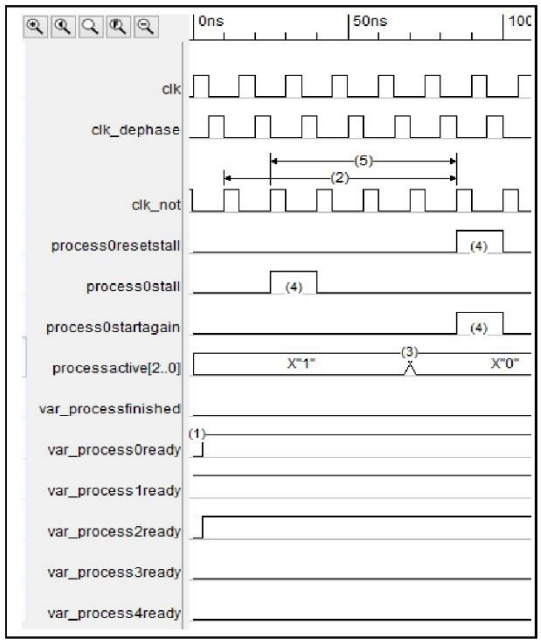

Fig. 5. Time for a task switch

The algorithm, shown in the Fig. 3, will ensures the execution of each task, even for those states that are different from normal state, only if the occurrence of the tasks and the time for the TRB is chosen properly.

If these two requirements are not met, the scheduler will not work properly because one of the two unfortunate situations, explained above, will happen. This situation is not a consequence of the scheduling algorithm being implemented in hardware, the same situation could happened to a scheduling algorithm implemented in software. The conclusion from [9] persist in this paper, even though exists the situation explained above. The nMPRA microcontroller provides very good switching times, constant 5 machine cycles. Because the switch of the context and the critical sections are missing the current architecture is more robust and less susceptible to invalid data due to operating system context switch.

Acknowledgment

This paper was supported by the project "Sustainable performance in doctoral and post-doctoral research PERFORM - Contract no. POSDRU/159/1.5/S/138963", project co-funded from European Social Fund through Sectorial Operational Program Human Resources 2007-2013.

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Proceedings of
2014 18th International Conference on
System Theory, Control and Computing (ICSTCC)

(Joint conference SINTES 18, SACCS 14, SIMSIS 18)

October 17 - 19, 2014

Editors:
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ISBN 978-1-4799-4602-0

18th International Conference on System Theory, Control and Computing

October 17-19, 2014, Sinaia, Romania

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Program at a Glance

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09:20-10:05 Miorita Plenary Session FrPP1 *Perspectives on Software Integration for Intelligent Robotic Systems*				
10:05-10:50 Miorita Plenary Session FrPP2 *Visual Data Understanding and UI Control with Humans in the Loop*				
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Miorita
Plenary Session SuPCC

Closing Ceremony

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Technical Program for Friday October 17, 2014

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FrPOC Plenary Session, Miorita

Opening Ceremony

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Co-Chair: Rasvan, Vladimir — Univ. of Craiova

FrPP1 Plenary Session, Miorita

Perspectives on Software Integration for Intelligent Robotic Systems

Cervera, Enric — Jaume-I Univ. of Castello de la Plana

Chair: Rasvan, Vladimir — Univ. of Craiova

FrPP2 Plenary Session, Miorita

Visual Data Understanding and UI Control with Humans in the Loop

Charvillat, Vincent — Univ. of Toulouse

Chair: Lazar, Corneliu — Gheorghe Asachi Tech. Univ. of Iasi

FrPP3 Plenary Session, Miorita

How to Cluster Data: Algorithms and Validation

Fränti, Pasi — Univ. of Eastern Finland

Chair: Minzu, Viorel — Dunarea de Jos Univ. of Galati

FrA1 Regular Session, Miorita

Linear Systems

Chair: Oara, Cristian — Pol. Univ. of Bucharest
Co-Chair: Pastravanu, Octavian-Cezar — Gheorghe Asachi Tech. Univ. of Iasi

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On a Conjecture in Stability Analysis of Polytopic Systems – Mimicking Spectral Radius Properties from Real to Complex Matrices

Pastravanu, Octavian-Cezar — Gheorghe Asachi Tech. Univ. of Iasi
Matcovschi, Mihaela-Hanako — Gheorghe Asachi Tech. Univ. of Iasi

11:30-11:50, Paper FrA1.2

Study of the Interaction between a One Degree of Freedom Force Augmenting Device and a Human Operator

Gadi, Suresh Kumar — Pol. Univ. of Aguascalientes
Osorio-Cordero, Antonio — Cinvestav

Lozano, Rogelio — Univ. of Tech. of Compiègne

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Minimal Factorization of Transfer Matrices for Generalized Systems

Flutur, Cristian — Pol. Univ. of Bucharest

Oara, Cristian — Pol. Univ. of Bucharest

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Sufficient Conditions for Stabilisability of Decentralised LTI Systems: Weighted Directed Graph Approach

Abdolmaleki, Mohammad — Univ. of Melbourne

Aldeen, Mohammad — Univ. of Melbourne

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Outer Bound Estimations for the Spectral Radii of Interval Matrices

Matcovschi, Mihaela-Hanako — Gheorghe Asachi Tech. Univ. of Iasi

Pastravanu, Octavian-Cezar — Gheorghe Asachi Tech. Univ. of Iasi

Voicu, Mihail — Gheorghe Asachi Tech. Univ. of Iasi

FrA2 Regular Session, Ara

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Chair: Ungureanu, Florina — Gheorghe Asachi Tech. Univ. of Iasi

Co-Chair: Florea, Adrian — Lucian Blaga Univ. of Sibiu

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Buduleci, Claudiu-Raul — Lucian Blaga Univ. of Sibiu

Chiş, Radu — Tehnical Univ. of Cluj-Napoca

Gellert, Arpad — Lucian Blaga Univ. of Sibiu

Vintan, Lucian — Lucian Blaga Univ. of Sibiu

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Bozesan, Andreea — Pol. Univ. of Timisoara

Vladutiu, Mircea — Pol. Univ. of Timisoara

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Dual Priority Scheduling Algorithm Used in the Nmpra Microcontrollers

Andries, Lucian — Stefan Cel Mare Univ. of Suceava

Gaitan, Vasile Gheorghita — Stefan Cel Mare Univ. of Suceava

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Sensorial System for HYPER-REDUNDANT ARM

Vladu, Ionel Cristian — Univ. of Craiova

Vladu, Ileana — Univ. of Craiova

Ivanescu, Mircea — Univ. of Craiova
Strîmbeanu, Daniel — Univ. of Craiova

12:30-12:50, Paper FrA2.5

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Moisuc (Ciobanu), Elena-Eugenia — Stefan Cel Mare Univ. of Suceava
Larionescu, Alexandru-Bogdan — Stefan Cel Mare Univ. of Suceava
Ungurean, Ioan — Stefan Cel Mare Univ. of Suceava

FrA3 Invited Session, Carpati

Fractional Order Modeling and Control

Chair: Copot, Cosmin — Ghent Univ.
Co-Chair: Muresan, Cristina Ioana — Tech. Univ. of Cluj Napoca
Organizer: Copot, Cosmin — Ghent Univ.
Organizer: Muresan, Cristina Ioana — Tech. Univ. of Cluj-Napoca

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Folea, Silviu — Tech. Univ. of Cluj-Napoca
Marton, Botond — Tech. Univ. of Cluj-Napoca
Muresan, Cristina Ioana — Tech. Univ. of Cluj-Napoca

11:30-11:50, Paper FrA3.2

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Rapaić, Milan — Univ. of Novi Sad
Šekara, Tomislav — Univ. of Belgrade
Jelicic, Zoran — Univ. of Novi Sad

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Visual Servo Control of a Steward Platform Using Fractional-Order PID Controller (I)

Copot, Cosmin — Ghent Univ.
Ionescu, Clara — Ghent Univ.
De Keyser, Robin M.C. — Ghent Univ.

12:10-12:30, Paper FrA3.4

Fractional Order Control on a Wind Turbine Benchmark (I)

Viveiros, Carla — Inst. Superior De Engenharia De Lisboa
Melicio, Rui — Univ. De Evora
Igreja, José Manuel Cardoso — Inst. Superior De Engenharia De Lisboa
Mendes, Victor — Inst. Superior De Engenharia De Lisboa

12:30-12:50, Paper FrA3.5

Benign and Malignant Breast Tumors: Diagnosis Using Fractal Measures (I)

Dobrescu, Radu — Pol. Univ. of Bucharest

Ichim, Loretta — Pol. Univ. of Bucharest
Mocanu, Stefan — Pol. Univ. of Bucharest
Popescu, Dan — Pol. Univ. of Bucharest

FrA4 Regular Session, Laca
Optimisation

Chair: Shcherbakov, Pavel — Moscow Inst. for Control Sciences, RAS
Co-Chair: Caruntu, Constantin - Florin — Gheorghe Asachi Tech. Univ. of Iasi

11:10-11:30, Paper FrA4.1
Precedence Constraints Treatment in Ant Colony Optimization
Serbencu, Adrian Emanoil — Dunarea De Jos Univ. of Galati
Minzu, Viorel — Dunarea De Jos Univ. of Galati
Serbencu, Adriana — Dunarea De Jos Univ. of Galati

11:30-11:50, Paper FrA4.2
On the Computation of Lyapunov Functions for Discrete-Time Nonlinear Systems
Bobiti, Ruxandra Valentina — Eindhoven Univ. of Tech
Lazar, Mircea — Eindhoven Univ. of Tech

11:50-12:10, Paper FrA4.3
Optimal Control with Fixed-End Point for Linear Perturbed Systems
Ostafi, Florin — Gheorghe Asachi Tech. Univ. of Iasi
Botan, Corneliu — Gheorghe Asachi Tech. Univ. of Iasi

12:10-12:30, Paper FrA4.4
Quadratic Image of a Ball: Towards Efficient Description of the Boundary
Polyak, Boris T. — Moscow Inst. for Control Sciences
Shcherbakov, Pavel — Moscow Inst. for Control Sciences
Khlebnikov, Mikhail — Moscow Inst. for Control Sciences

12:30-12:50, Paper FrA4.5
Trajectory Planner for Mobile Robots Using Particle Swarm Optimization
Solea, Razvan — Dunarea De Jos Univ. of Galati
Cernega, Daniela Cristina — Dunarea De Jos Univ. of Galati

FrA5 Regular Session, Bucegi 1
Software Engineering

Chair: Iliescu, Dragos — Univ. Pol. of Bucharest
Co-Chair: Costeniuc, George — Continental Automotive Romania SRL Iasi

11:10-11:30, Paper FrA5.1
Is FBDK Suitable for Developing and Implementing Process Control Optimization Problems?
Rohat, Oana — Pol. Univ. of Bucharest
Popescu, Dan — Pol. Univ. of Bucharest

11:30-11:50, Paper FrA5.2

Double Precision Stencil Computations on Kepler GPUs

Vizitiu, Anamaria	Transilvania Univ. of Brasov
Itu, Lucian	Lucian Blaga Univ. of Sibiu
Lazar, Laszlo	SC Siemens SRL
Suciu, Constantin	SC Siemens SRL

11:50-12:10, Paper FrA5.3

Assisted Management of Product Data - a PDM Application Proposal

Iliescu, Dragos	Pol. Univ. of Bucharest
Ciocan, Ion	Pol. Univ. of Bucharest
Mateias, Ion	Doosan IMGB Bucharest

12:10-12:30, Paper FrA5.4

Semantic Report Search Engine - Questor

Vasilateanu, Andrei	Pol. Univ. of Bucharest
Goga, Nicolae	Pol. Univ. of Bucharest
Moldoveanu, Alin	Pol. Univ. of Bucharest

12:30-12:50, Paper FrA5.5

SaaS Solutions for Small-Medium Businesses Developer's Perspective on Creating New SaaS Products

Resceanu, Ionut Cristian	Univ. of Craiova
Resceanu, Cristina Floriana	Univ. of Craiova
Simionescu, Sabin Mihai	SC White Pyramid SRL

FrB1 Invited Session, Miorita

New Trends in Robotic Systems

Chair: Cervera, Enric	Jaume-I Univ. of Castello de la Plana
Co-Chair: Panescu, Doru-Adrian	Gheorghe Asachi Tech. Univ. of Iasi
Organizer: Cervera, Enric	Jaume-I Univ. of Castello de la Plana
Organizer: Borangiu, Theodor	Pol. Univ. of Bucharest
Organizer: Panescu, Doru-Adrian	Gheorghe Asachi Tech. Univ. of Iasi
Organizer: Burlacu, Adrian	Gheorghe Asachi Tech. Univ. of Iasi

16:10-16:30, Paper FrB1.1

Integration of Mobile Agents in Distributed Manufacturing Control (I)

Raileanu, Silviu	Pol. Univ. of Bucharest
Borangiu, Theodor	Pol. Univ. of Bucharest
Ivanescu, Nick Andrei	Pol. Univ. of Bucharest
Morariu, Octavian	Pol. Univ. of Bucharest

16:30-16:50, Paper FrB1.2

Trading Optimality for Computational Feasibility in a Sample Gathering Problem (I)

Kloetzer, Marius	Gheorghe Asachi Tech. Univ. of Iasi
Ostafi, Florin	Gheorghe Asachi Tech. Univ. of Iasi
Burlacu, Adrian	Gheorghe Asachi Tech. Univ. of Iasi

16:50-17:10, Paper FrB1.3

A Constraint Satisfaction Approach for Planning of Multi-Robot Systems (I)

Panescu, Doru-Adrian	Gheorghe Asachi Tech. Univ. of Iasi
Pascal, Carlos	Gheorghe Asachi Tech. Univ. of Iasi

17:10-17:30, Paper FrB1.4

Spiking Neural Network for Controlling the Artificial Muscles of a Humanoid Robotic Arm (I)

Hulea, Mircea	Gheorghe Asachi Tech. Univ. of Iasi
Caruntu, Constantin - Florin	Gheorghe Asachi Tech. Univ. of Iasi

17:30-17:50, Paper FrB1.5

3D Complex Surface Generation through Procedural Robot Motion (I)

Borangiu, Theodor	Pol. Univ. of Bucharest
Ciocan, Mihai	Pol. Univ. of Bucharest
Raileanu, Silviu	Pol. Univ. of Bucharest
Morariu, Octavian	Pol. Univ. of Bucharest
Stocklosa , Octavian	Pol. Univ. of Bucharest

17:50-18:10, Paper FrB1.6

Kinematic Evaluation of Articulated Rigid Objects (I)

Burlacu, Adrian	Gheorghe Asachi Tech. Univ. of Iasi
Condurache, Daniel	Gheorghe Asachi Tech. Univ. of Iasi
Clim, Eduard	Gheorghe Asachi Tech. Univ. of Iasi

FrB2 Invited Session, Ara

Real Time Systems Applications

Chair: Popescu, Dumitru	Pol. Univ. of Bucharest
Co-Chair: Lupu, Ciprian	Pol. Univ. of Bucharest
Organizer: Popescu, Dumitru	Pol. Univ. of Bucharest
Organizer: Lupu, Ciprian	Pol. Univ. of Bucharest

16:10-16:30, Paper FrB2.1

Emergent Intelligence in Agents: A Scalable Architecture for Smart Cities (I)

Patrascu, Monica	Pol. Univ. of Bucharest
Dragoicea, Monica	Pol. Univ. of Bucharest
Ion, Andreea	Pol. Univ. of Bucharest

16:30-16:50, Paper FrB2.2

Real Time Agent Based Simulation for Smart City Emergency Protocols (I)

Dragoicea, Monica	Pol. Univ. of Bucharest
Patrascu, Monica	Pol. Univ. of Bucharest
Serea, George Alexandru	Pol. Univ. of Bucharest

16:50-17:10, Paper FrB2.3

An Approach for Load Balancing in Virtual Power Plant Structures (I)

Lupu, Ciprian	Pol. Univ. of Bucharest
Oancea, Dumitru	Pol. Univ. of Bucharest

Oara, Cristian	Pol. Univ. of Bucharest
Lupu, Mircea	Transilvania Univ. of Brasov
Apetrei, Dan	ELSACO Energy

17:10-17:30, Paper FrB2.4

Real-Time Acquisition of Quality Verified Nonstandardized Color Images for Skin Lesions Risk Assessment – a Preliminary Study (I)

Udrea, Andreea	Pol. Univ. of Bucharest
Lupu, Ciprian	Pol. Univ. of Bucharest

17:30-17:50, Paper FrB2.5

Designing Control Systems with Distributed Parameters (I)

Miron, Cristian	Pol. Univ. of Bucharest
Popescu, Dumitru	Pol. Univ. of Bucharest
Petrescu, Catalin	Pol. Univ. of Bucharest

17:50-18:10, Paper FrB2.6

Fuzzy Modeling and Control for a Road Section (I)

Dimon, Catalin	Pol. Univ. of Bucharest
Popescu, Dumitru	Pol. Univ. of Bucharest
Stefanoiu, Dan	Pol. Univ. of Bucharest

FrB3 Regular Session, Carpati

Applied Informatics

Chair: Postolache, Mihai	Gheorghe Asachi Tech. Univ. of Iasi
Co-Chair: Ciobanu, Adrian	Inst. of Computer Science, Romanian Acad. Iasi Branch

16:10-16:30, Paper FrB3.1

A Review of HDL-Based System for Real-Time Image Processing Used in Tumors Screening

Chiuchisan, Iuliana	Stefan Cel Mare Univ. of Suceava
Geman, Oana	Stefan Cel Mare Univ. of Suceava

16:30-16:50, Paper FrB3.2

A Study on Automatic Recognition of Positive and Negative Emotions in Speech

Pavaloi, Ioan	Inst. of Computer Science, Romanian Acad. Iasi Branch
Ciobanu, Adrian	Inst. of Computer Science, Romanian Acad. Iasi Branch
Luca, Mihaela	Inst. of Computer Science, Romanian Acad. Iasi Branch
Musca, Elena	Inst. of Computer Science, Romanian Acad. Iasi Branch
Barbu, Tudor	Inst. of Computer Science, Romanian Acad. Iasi Branch
Ignat, Anca	Alexandru Ioan Cuza Univ. of Iasi

16:50-17:10, Paper FrB3.3

Security Solution for Healthcare Hybrid Cloud Platform

Marcu, Roxana Elena	Pol. Univ. of Bucharest

17:10-17:30, Paper FrB3.4

Uniformity and Correlation Test Parameters for Random Numbers Generators

Petrila, Iulian — Gheorghe Asachi Tech. Univ. of Iasi

Manta, Vasile — Gheorghe Asachi Tech. Univ. of Iasi

Ungureanu, Florina — Gheorghe Asachi Tech. Univ. of Iasi

17:30-17:50, Paper FrB3.5

Artificial Intelligence Application Built for ATS Detection with a New Portable Hollow Fiber IRAS Spectrometer

Praisler, Mirela — Dunarea De Jos Univ. of Galati

Ciochina, Stefanut — Dunarea De Jos Univ. of Galati

Stoica, Atanasia — Dunarea De Jos Univ. of Galati

17:50-18:10, Paper FrB3.6

CFD Simulation of the Airflow Pattern within a Three-Bed Hospital Room with or without a Portable Air Conditioner in Use

Vladut, Gabriel — S.C. IPA CIFATT Craiova

Sbirna, Liana Simona — Univ. of Craiova

Sbirna, Sebastian — St. Stephen Ec. School of Craiova

Codresi, Cristian — Sodinal Romania

Martin, Liviu — Turceni City Hospital

FrB4 Regular Session, Laca

Control Applications

Chair: Valean, Honoriu — Tech. Univ. of Cluj-Napoca

Co-Chair: Nitulescu, Mircea — Univ. of Craiova

16:10-16:30, Paper FrB4.1

Dynamics Properties and Control for Oilwell Drillstrings

Bobasu, Eugen — Univ. of Craiova

Ivanov, Sergiu — Univ. of Craiova

Popescu, Dan — Univ. of Craiova

Rasvan, Vladimir — Univ. of Craiova

16:30-16:50, Paper FrB4.2

The Determination of the Maximum Energetic Zones for a Wind System, Operating at Variable Wind Speeds

Erdodi, Gheza-Mihai — Pol. Univ. of Timisoara

Petrescu, Doru-Ionut — Pol. Univ. of Timisoara

Sorandaru, Ciprian — Pol. Univ. of Timisoara

Musuroi, Sorin — Pol. Univ. of Timisoara

16:50-17:10, Paper FrB4.3

Modelling of Bio-Products Conversion Processes for Pollutant Compounds Formation Dynamics Assessment

Roman, Monica — Univ. of Craiova

Selisteanu, Dan — Univ. of Craiova

17:10-17:30, Paper FrB4.4

Parameter Estimation Techniques for a Rehabilitation Hand Exoskeleton

Ivanescu, Mircea	Univ. of Craiova
Popescu, Dorin	Univ. of Craiova
Nitulescu, Mircea	Univ. of Craiova
Popescu, Nirvana	Pol. Univ. of Bucharest

17:30-17:50, Paper FrB4.5

Temperature Control of the Asphaltic Emulsion in an Industrial Tank

Muresan, Vlad	Tech. Univ. of Cluj-Napoca
Abrudean, Mihail	Tech. Univ. of Cluj-Napoca
Valean, Honoriu	Tech. Univ. of Cluj-Napoca
Colosi, Tiberiu	Tech. Univ. of Cluj-Napoca

17:50-18:10, Paper FrB4.6

Variable DC Power Sources for 13C Isotope Separation Column Boiler Supply

Dulf, Eva Henrietta	Tech. Univ. of Cluj Napoca
Both, Roxana	Tech. Univ. of Cluj-Napoca
Munteanu, Radu A.	Tech. Univ. of Cluj-Napoca
Festila, Clement	Tech. Univ. of Cluj Napoca
Secara, Mihai	Tech. Univ. of Cluj-Napoca

FrB5 Regular Session, Bucegi 1

Nonlinear Systems

Chair: Sima, Vasile	National Inst. for Res. and Development in Informatics, Bucharest
Co-Chair: Halas, Miroslav	Slovak Univ. of Tech.

16:10-16:30, Paper FrB5.1

Modelling and Performance Analysis of an Urban Wastewater Treatment Plant

Luca, Laurentiu	Dunarea De Jos Univ. of Galati
Barbu, Marian	Dunarea De Jos Univ. of Galati
Caraman, Sergiu	Dunarea De Jos Univ. of Galati

16:30-16:50, Paper FrB5.2

Eigenvalues for a Nonlinear Time-Delay System

Halas, Miroslav	Slovak Univ. of Tech. in Bratislava

16:50-17:10, Paper FrB5.3

Control-Oriented Modeling and Flight Dynamics Analysis of a Flexible Generic Hypersonic Vehicle

Zhu, Jiao	Beihang Univ
Chen, Wanchun	Beihang Univ
Ma, Hongzhong	Beijing Electro-Mechanical Engineering Inst
Yang, Zhihong	Beijing Aerospace Tech. Inst

17:10-17:30, Paper FrB5.4

Imperialist Competitive Algorithm with Variable Parameters for the Optimization of a Fuzzy Controller

Ciurea, Stelian	Lucian Blaga Univ. of Sibiu
Trifa, Viorel	Tech. Univ. of Cluj-Napoca

17:30-17:50, Paper FrB5.5

Nonlinear Fuzzy Control of Human Heart Rate During Aerobic Endurance Training with Respect to Significant Model Variations

Patrascu, Adrian	Babes-Bolyai Univ. of Cluj-Napoca
Patrascu, Monica	Pol. Univ. of Bucharest
Hantiu, Iacob	Babes-Bolyai Univ. of Cluj-Napoca

17:50-18:10, Paper FrB5.6

Sampled-Data Robust Feedback Linearization Using Neural Network-Aided Unscented Kalman Filter

Zaheer, Asim	National Univ. of Sciences and Tech. of Islamabad
Hasan, Momena	National Univ. of Sciences and Tech. of Islamabad
Ali, Usman	National Univ. of Sciences and Tech. of Islamabad
Salman, Muhammad	National Univ. of Sciences and Tech. of Islamabad

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