Hardware Event Treating in *nMPRA*

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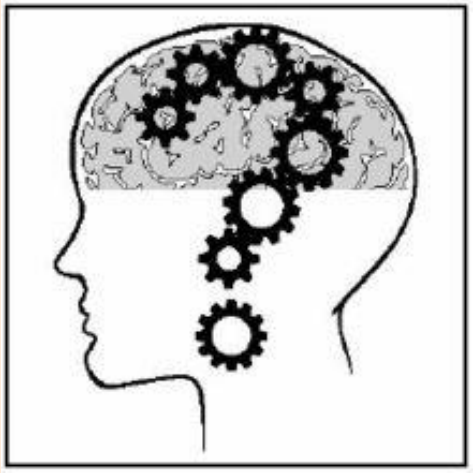
This paper was supported by the project "Sustainable performance in doctoral and post-doctoral research PERFORM–Contract no. POSDRU/159/ 1.5/S/138963", project co-funded from European Social Fund through Sectorial Operational Program Human Resources 2007-2013.

12th International Conference on DEVELOPMENT AND APPLICATION SYSTEMS
Suceava, Romania, May 15-17, 2014

INTRODUCTION

Events in RTS (*R*eal *T*ime *S*ystems):

- time events
- watchdog timer events
- deadline events
- interrupt events
- mutex events
- synchronization and inter-task communication events



PRESENTATION

Method of global prioritization of the events

- Using a hardware prioritization scheme for the *n-task* Multi Pipeline Register Architecture (***nMPRA***)

Analysis: How are treated mutex and inter-task communication events

- Using the same architecture

PROBLEM #1

RTOS FOR EMBEDDED SYSTEM

Can’t allow a task to synchronize simultaneously with multiple events utilized for resource sharing, synchronization and communication between tasks such as semaphores, flags, mutexes, signals, events, messages.

PROBLEM #2

GENERAL-PURPOSE PROCESSORS FOR EMBEDDED SYSTEMS

Inefficient power consumption and non-deterministic performances ⟶ Use of an oversized platform ⟶ are not suitable for embedded systems with low power consumption requirements and real-time capabilities

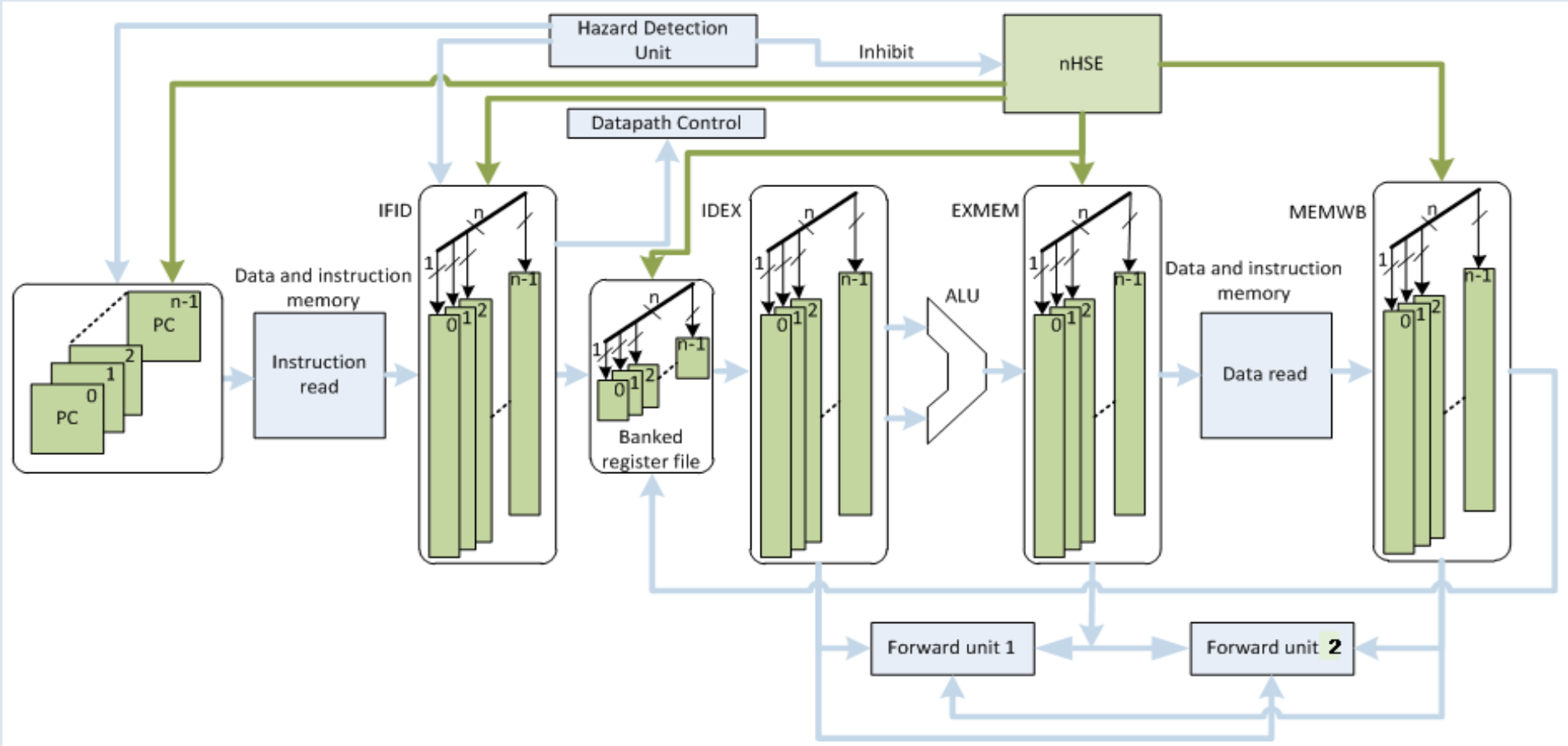
SOLUTIONS

Hardware Event Treating in *nMPRA*

- **Section II –** The *nMPRA* and its main features;
- **Section III –** the global prioritization of the events by category, using a hardware prioritization scheme;
- **Section IV –** an analysis of the treating of the synchronization and communication events, as well as the mutex events;
- **Section V –** the final conclusions.

nMPRA

- a hardware implemented support for event prioritization and treating
- MPRA ⟹ n-task MPRA (*nMPRA*): to replicate the pipeline registers; to create multiple instances of the CPU ⟹ *semi CPU* for every *task i* (*sCPU*$_i$)



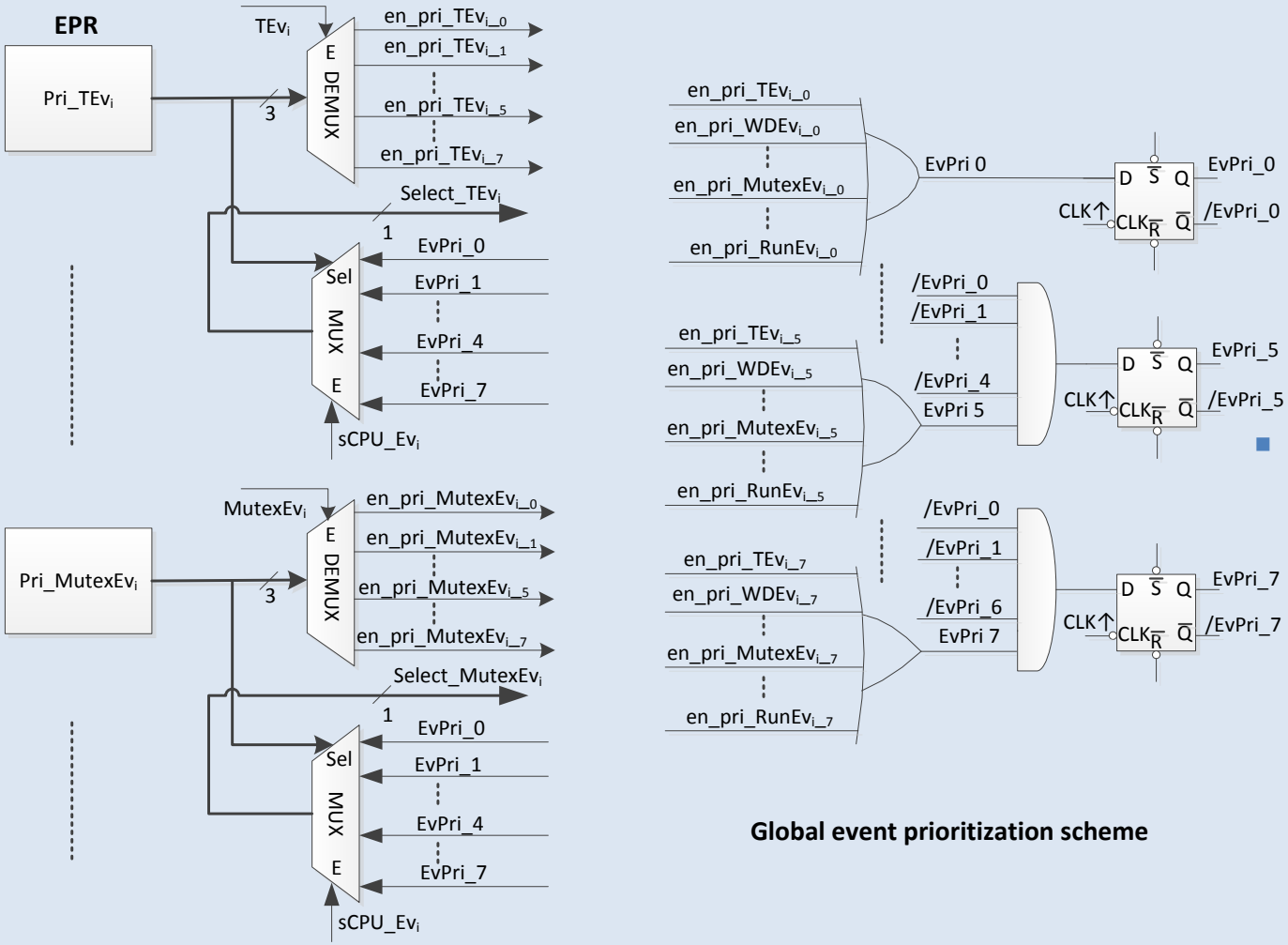
The *nMPRA* ⟶ an original hardware structure utilized for task scheduling, both static and dynamic, and provides unitary events management.

WHAT WE AIM FOR

- to improve through hardware the performances of RTOS for microcontrollers
- to switch faster between the tasks
- to improve the response time to external events
- to improve the behavior of the interrupts, which are treated as events in this case
- to offer several types of inter-process communication primitives (messages, mutexes, and so on)

Global Events Prioritization

- every $sCPU_i$ has attached an **E**vent **P**riority **R**egister (EPR_i), which contains the priority level of each type of event associated with that $sCPU_i$
- the priority is different for each type of events



Global event prioritization scheme

- The prioritization scheme selects the active event category with the highest priority, in order to be treated

- The priority level of each event category can be static or it can be changed dynamically, depending on the system's demands.
- If there are multiple active events in the selected category, it must be done another selection of the event from that category that will actually be treated first.
- This second selection depends on the type of the event category.

Analisys of the Syn and Mutex Events

- The ***E**vent **R**egister **F**ile* (**ERF**) consists of *s* registers of *2n+k+1* bits, storing the event itself on the most significant bit.
- Writing an event in ERF will be done at the first free address determined by the hardware scheme.
- In the service routine of the *syn* events we'll have to search the ERF and read all the events associated with task *i* and then clear them.
- The priority of the *syn* events is given by their position in the ERF.

- The mutexes are implemented using a set of global registers with fast access.
- The ***M**utex **R**egister **F**ile* (**MRF**) is composed from *m* registers with length *n*+1 bits that contain the *mutex* bit in the highest bit position and the ID of the proprietary task that holds the mutex in the lowest priority *n* bits.
- The **MRF** registers can be accessed by any $sCPU_i$ and this means they are a shared resource for all $sCPU_i$ in the system. Any time a blocked mutex gets freed, it activates the $MutexEv_i$ signal.

CONCLUSIONS

- The hardware treating of the events, reducing the time necessary to identify the source of the event and to launch the appropriate event servicing routine.
- The prioritization scheme is simple and can be applied to all the events.
- It can be implemented for other event categories.

FUTURE PAPERS

- The structure of the PC_i registers
- The structure of the trap registers
- The mechanism that allows the automatic loading of the procedures' address
- The structure of the pointer registers
- The analysis of other events.

Proceedings of the

2014 International Conference on Development and Application Systems (DAS)

12th Edition, May 15-17, 2014, Suceava, Romania

Universitatea Ştefan cel Mare Suceava

Stefan cel Mare University of Suceava
Faculty of Electrical Engineering and Computer Science
www.dasconference.ro

IEEE Catalog Number CFP1465Y-DVD

ISBN 978-1-4799-5092-8

CONTENTS

SECTION A - Systems, Process Control and Automations

Embedded Networked Monitoring and Control for Renewable Energy Storage Systems
Grigore STAMATESCU, Iulia STAMATESCU, Nicoleta ARGHIRA, Ioana FAGARASAN, Sergiu Stelian ILIESCU 1

PID-Controller Application in the System for Variable Technological Process
Simion BARANOV, Irina COJUHARI, Ion FIODOROV, Leonid GORCEAC 7

Improving Interrupt Handling in the nMPRA
Nicoleta Cristina GAITAN, Vasile Gheorghita GAITAN, Elena-Eugenia (CIOBANU) MOISUC 11

Fuzzy Decision Support System for Solar Tracking Optimization
Iulia STAMATESCU, Grigore STAMATESCU, Nicoleta ARGHIRA, Ioana FAGARASAN, Sergiu Stelian ILIESCU 16

Real-Time Reconfiguration of Distributed Control System Based on Hard Petri Nets
Victor ABABII, Viorica SUDACEVSCHI, Marin PODUBNII, Irina COJUHARI 21

On Quick-Change Detection based on Process Adaptive Modelling and Identification
Dorel AIORDACHIOAIE 25

Experimental Analysis on a Self Excited Induction Generator for Standalone Wind Electric Pumping Stations
Mohamed BARARA, Ahmed ABBOU, Mohamed AKHERRAZ, Abderrahim BENNASSAR, Silviu IONITA, Emilian LEFTER, Bogdan ENACHE 29

Optimal Estimation of Parameters in Systems with the Phase Space Variable Measurability
Mykola ILASHCHUK, Eugene SOPRONIUK 37

Principle of Maximum to Control Systems with Delay and Change of Phase Space Measurability
Tetiana HABUZA, Fedir SOPRONIOUK 43

Robotic Arm Control in 3D Space Using Stereo Distance Calculation
Roland SZABO, Aurel GONTEAN 50

SECTION B - Communications and Computer Networks

Matlab Based Platform for the Evaluation of Modulation Techniques Used in VLC
Steven De LAUSNAY, Lieven De STRYCKER, Jean-Pierre GOEMAERE, Nobby STEVENS, Bart NAUWELAERS 57

Optimization of an Improved Nyquist Filter With Piece-Wise Polynomial Frequency Characteristic
Nicolae Dumitru ALEXANDRU, Alexandra Ligia BALAN 62

Hardware Event Treating in nMPRA
Elena-Eugenia (CIOBANU) MOISUC, Alexandru-Bogdan LARIONESCU, Vasile Gheorghita GAITAN 66

Sensors Network Based on Mobile Robots
Victor ABABII, Viorica SUDACEVSCHI, Marin PODUBNII, Irina COJUHARI 70

Using dual priority scheduling to improve the resource utilization in the nMPRA microcontrollers
Nicoleta Cristina GAITAN, Lucian ANDRIES 73

Introducing aceMote: an energy efficient 32 bit mote
Andrei STAN, Nicolae BOTEZATU 79

Evaluation of the noise effects on Visible Light Communications using Manchester and Miller coding
Alin-Mihai CAILEAN, Barthelemy CAGNEAU, Luc CHASSAGNE, Valentin POPA, Mihai DIMIAN 85

Implementation and Performance Analysis of Zero Forcing MIMO Detection Algorithm
Vakulabharanam RAMAKRISHNA, Tipparti Anil KUMAR 90

Design of a Multi-Input-Multiple-Output Visible Light Communication System for Transport Infrastructure to Vehicle Communication
Lucian-Nicolae COJOCARIU, Valentin POPA 93

SECTION C - Electronics and Computer Aided Engineering

Eddy Current Nondestructive Evaluation – the Challenge of Accurate Modeling
Nathan IDA 97

Using a Decision Tree for Real-Time Distributed Indoor Localization in Healthcare Environments
Jeroen WYFFELS, Jos De BRABANTER, Jean-Pierre GOEMAERE, Bart NAUWELAERS, Lieven De STRYCKER, Piet VERHOEVE, Pieter CROMBEZ 103

A 2.4 GHz Phase Locked Loop for a Linear Phased Antenna Array
Anneleen Van NIEUWENHUYSE, Frederic TORREELE, Jean-Pierre GOEMAERE, Lieven De STRYCKER, Bart NAUWELAERS 110

A Comparison between Coded-Decoded Mode Signals on Multifunctional Registers
Mihai TIMIS, Alexandru VALACHI, Petru CASCAVAL, Radu SILION 116

Size, Shape and Temperature Effects on Ferro/Antiferro-electric Hysteresis Loops from Monte Carlo Simulations on 2D Ising Model
Daniel CHIRUTA, Christian CHONG, Pierre-Richard DAHOO, Yasser ALAYLI, Mihai DIMIAN, Jorge LINARES 122

A Study on Light Energy Harvesting from Indoor Environment
Aurel CHIRAP, Valentin POPA, Eugen COCA, Alin Dan POTORAC 127

The Temperature Dependence of Magnetostatic Interactions in Nanowire Systems
Andrei DIACONU, Ioan DUMITRU, Alexandru STANCU, Leonard SPINU 132

Multi-Inverter Six-Phase Motor Drive with Two DC Sources and Voltage Waveform Symmetries
Valentin OLESCHUK, Vladimir ERMURATSKII, Vladimir BERZAN 137