Improving Interrupt Handling in the nMPRA

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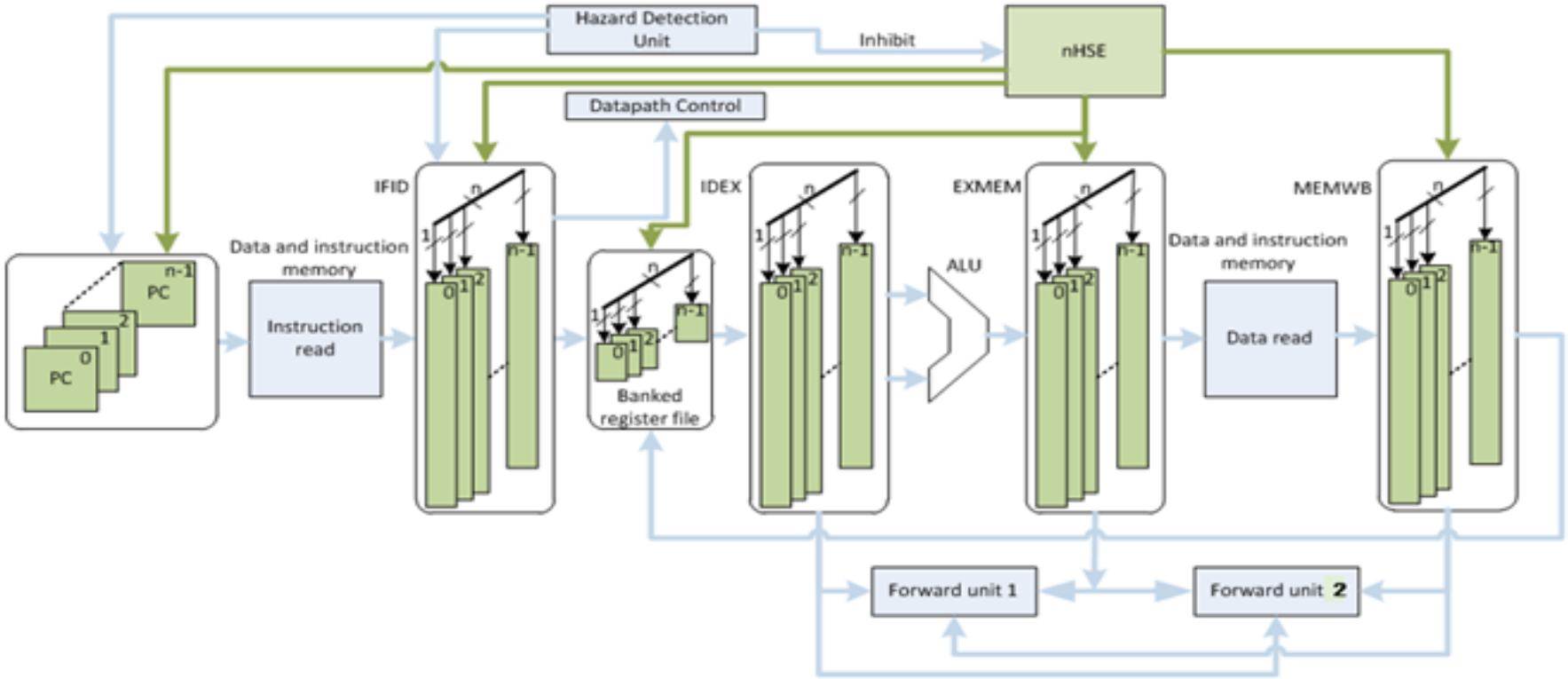
Contents

1. Introduction (1)

- The research presented in this paper is based on the functional Multi Pipeline Register Architecture (MPRA) processor which provides a very low time for the context switching operations as a consequence of the architecture concepts. This processor is capable to perform automatic context switching and to start the new task in a range of 1 to 3 clock cycles.

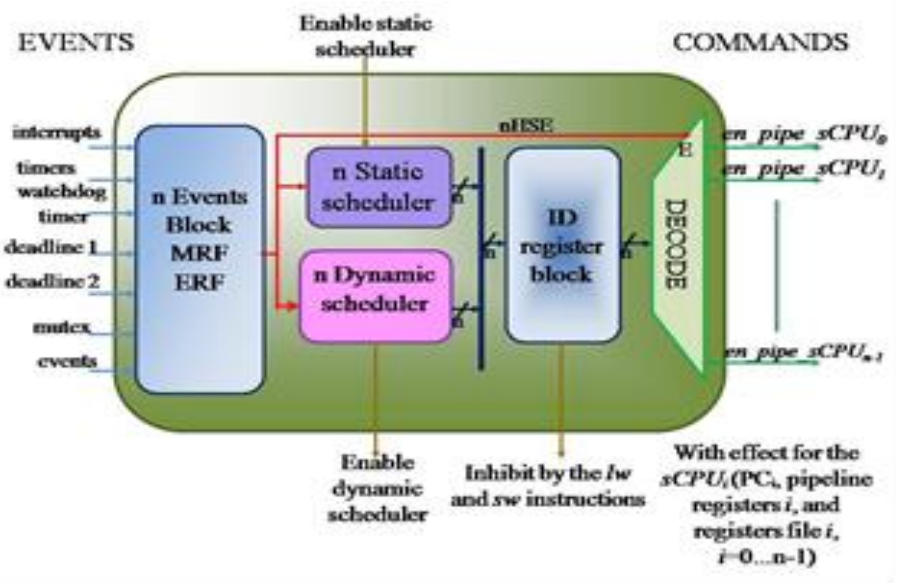
1. Introduction (2)



The context switching operations can be achieved in one processor cycle, and the response to an external event is delayed up to 1.5 processor cycles because each task has a set of pipeline.

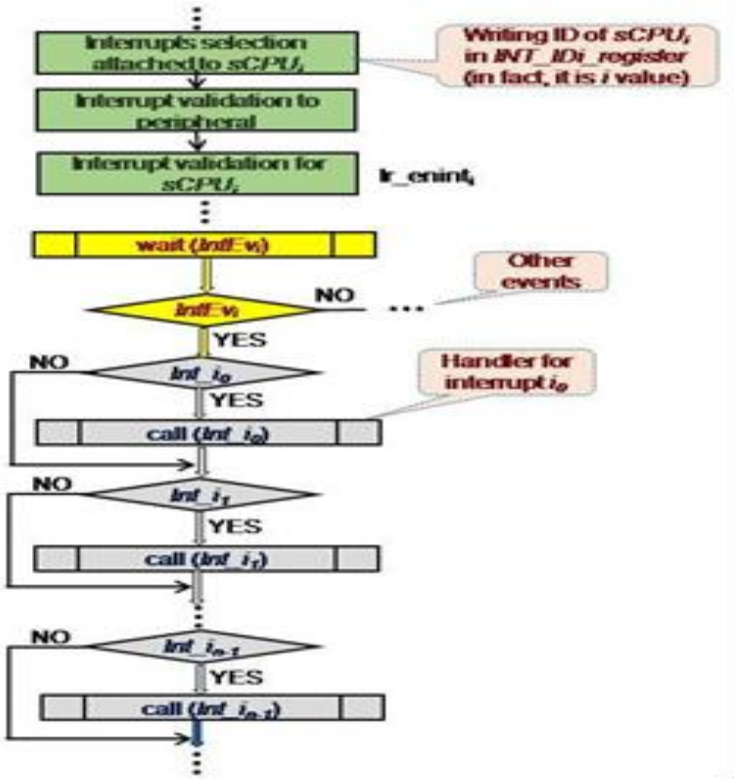
1. The nHSE architecture (1)

- The *nHSE* has input for events (interrupts, deadline, watchdog timers, timers, mutexes, message events, self-support event execution, as well enabling signals of static and dynamic schedulers and inhibiting the execution of load and store instructions) used to generate the $sCPU_i$ activation signals .



1. The nHSE architecture (3)

- The software solution it is simple (it does not require additional hardware modules) and versatile because the priorities of interrupts can be easily changed.



3. Conclusions (1)

- We improve the CPU architecture by an innovative solution for prioritization of the interrupts attached to the same task.

- Unlike loop testing solution, the proposed solution provides a uniform response time for any interrupt.

3. Conclusions (2)

- In the future, we will focus on the solution to create the priority encoder blocks depending on the number of attached interrupts and the possibility to upload direct to the CPU hardware the address of the interrupt handlers.

4. ACKNOWLEDGMENT

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CONTENTS

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SECTION C - Electronics and Computer Aided Engineering