

Study on Optimized Design of CPU Architecture Based Real-Time Scheduling and Pipeline Registers - PhD thesis summary

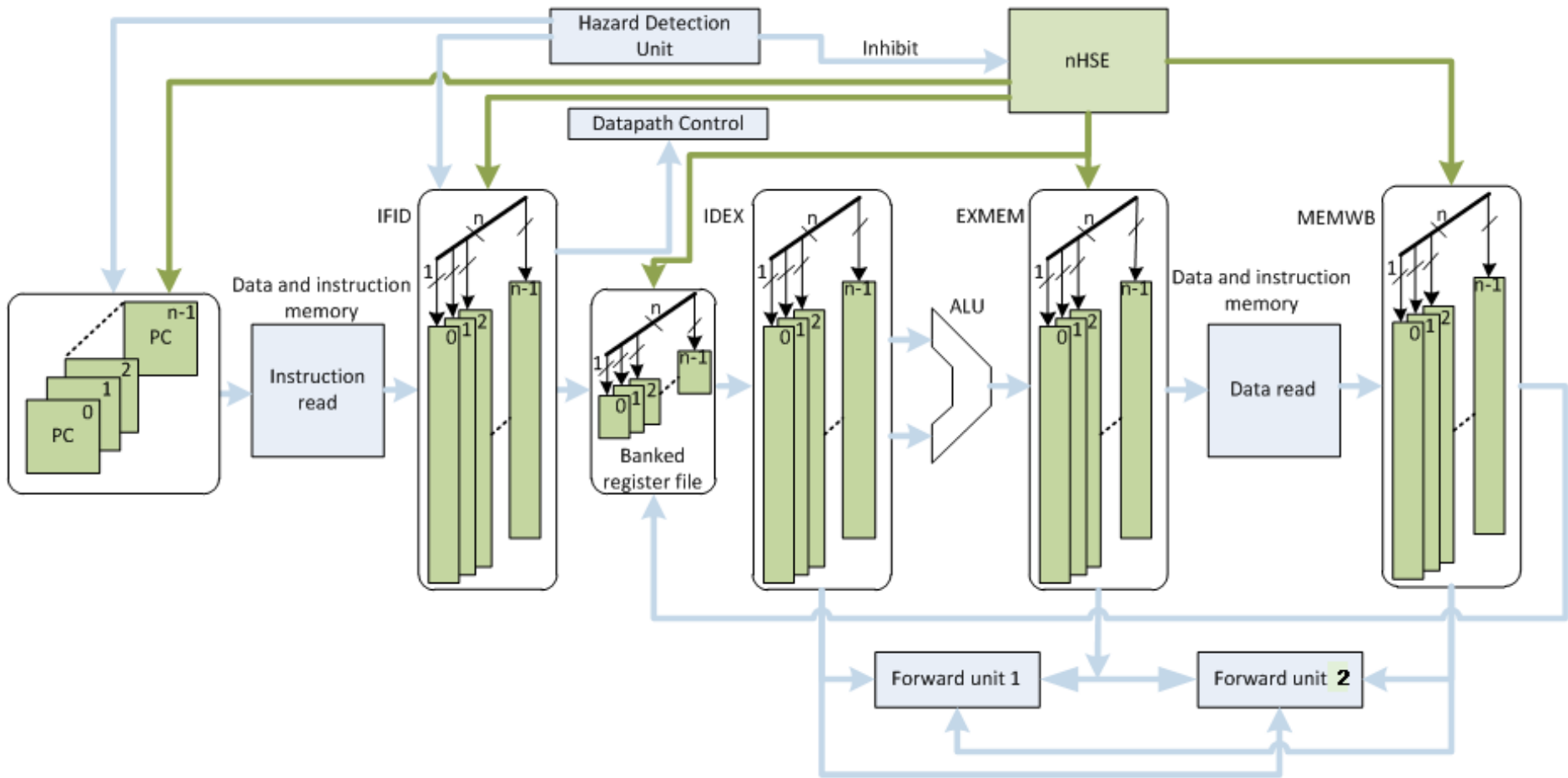
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THE STUDY PRESENTS

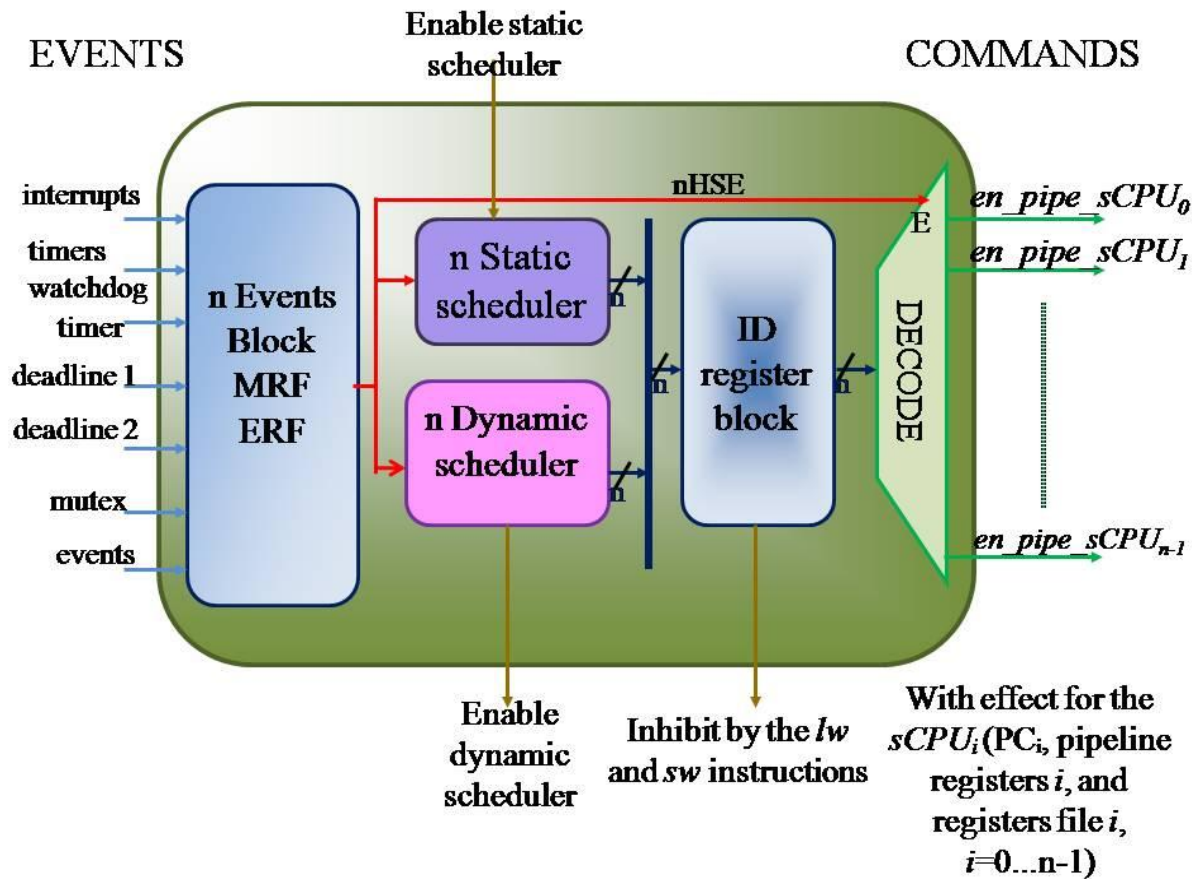


- A functional architecture of the processor
- MPRA: a multi-pipeline architecture → each task has its own set of pipeline registers
- Interrupt handling (the first part of the study) → the MPRA interrupts are viewed as tasks.



nMPRA

MPRA multiplied by n times \longrightarrow *nMPRA*

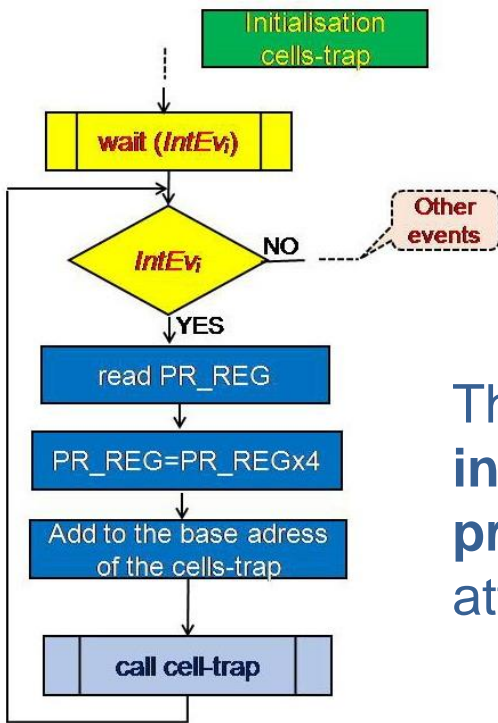


- **HSE** unit (**H**ardware **S**cheduler **E**ngine) is integrated into the processor.

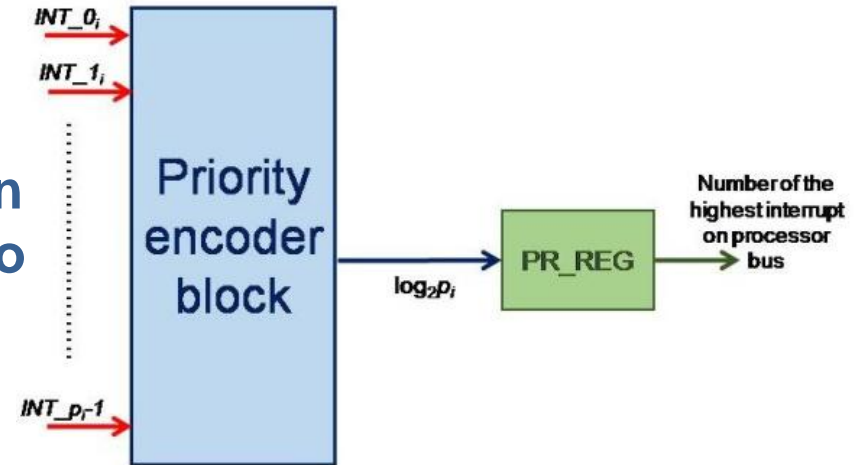
- **FPGA** (*Field Programmable Gate Array*) devices offer integrated elements of the complexity of the possible application oriented integrated circuits (ASIC - *Application Specific Integrated Circuit*), with **the advantage of programmability** or better said, of **configurability**.
- The architecture will be analyzed and implemented in **VHDL** with **FPGA Virtex6 a ML605** reference board produced by Xilinx.



CONCLUSIONS



The study proposed an innovative solution to prioritize interrupts attached to a task.



- there aren't specialized interrupts controller;
- interrupts inherit the priority task (sCPU);
- interrupt attached to a task can interrupt a lower-priority task but cannot interrupt the execution of the task who is attached, or higher-priority task;
- interrupt can be a task;
- all interrupts can be attached to a single task;
- interrupt doesn't reset another sCPU pipeline; the interrupts can be nested;
- interrupts priorities can be dynamic (by reattaching to a task, or by changing the priority of the task to which it is attached).

STUDIU ASUPRA ARHITECTURII OPTIMIZATE A UCP BAZATĂ PE PLANIFICARE REAL-TIME ȘI REGIȘTRI PIPELINE

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STUDY ON OPTIMIZED DESIGN OF CPU ARCHITECTURE BASED REAL-TIME SCHEDULING AND PIPELINE REGISTERS

ABSTRACT

The most effective interrupt handling is by hardware, which increases the speed of response to external events and reduces overhead. Therefore, the hardware method is used in most of the RTOS. Analyzing traditional models for interrupt management found their inability to provide the temporal determinism required in real-time systems. The study refers to the architecture of real-time architectures implemented in hardware, which obtain the available features of the operating system and their detection by hardware enabling. First, the study proposes Real Pipeline Register Architecture, which uses a unified space of pipeline for tasks and interrupts, as there must be an explicit hardware controller.

INTRODUCTION

The study presents a functional architecture of the processor, which provides very low existing times of critical functions of the way it is designed. This process, further research of E. Moisuc, E.S. Ciobanu, A. Ciobanu "Custom designed CPU architecture based on a hardware scheduler and independent pipeline registers - architecture description", 2012 12th International Conference on Information and Communication Technology Electronics and Information Science, October 2012 and E. Moisuc and E.S. Ciobanu "Custom designed CPU architecture based on a hardware scheduler and independent pipeline registers - concept and theory of operation", 2012 IEEE 2012 International Conference on Micro-Information Technology, September, IN, USA, 6-8 Sep 2012, ISBN: 978-1-4673-6936-2, 2200-2234 (2012), is capable of performing automatic switching events and to launch the next task in a single between 1 and 3 clock cycles. The processor implements a multiprocessor structure: pipeline registers and the registers and also an integrated hardware scheduler. The MPR is a multi-pipeline architecture, which means that each task has its own set of pipeline registers. Each unit (Hardware Scheduler Degree) is integrated into the processor. The MPR registers are viewed as tasks. The task part of the study concerned the interrupt handling. The used architecture is mMPRA - MPRAs realized by a team (E.S. Ciobanu, M.C. Ciobanu, I. Ciobanu, "CPU Architecture based on a Hardware Scheduler and Independent Pipeline Registers", submitted to IEEE Transactions on VLSI Systems, 2014), presented in Fig. 1. Because each task has its own set of pipeline registers and its own set of general registers, context switching can be done in one processor cycle, and the response to an external event may be delayed up to 3 processor cycles. For these reasons, the architecture is very fast. All tasks share other resources. An instance of this process can't call itself (recursion CPU for the task (acPU)) and perform a single task.

DEVELOPMENT

The mMPRA (Fig. 1) has an input such as events like interrupts, deadline, switching times, times, resource, message events, and support event generation, as well as reading signals of status and dynamic variables and inhibiting the execution of task and event continuation, generating acPU activation signals.



Fig. 1. mMPRA Architecture

MPRA enables activation or deactivation system interrupts. Interrupts follow the same procedure mentioned as tasks as their enabling or disabling their execution is done using the same instructions that are addressed to tasks. In the mMPRA, each time associated with a task can be configured to generate an interrupt when the time allocated to this task is coming completion. A task can respond to an external event if this event is masked by blocking and instructions.

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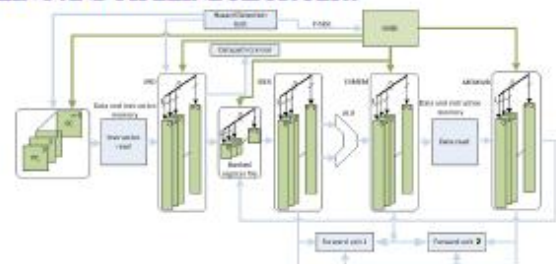


Fig. 2. mMPRA

The main instruction is very powerful because it allows synchronizing the execution while multiple events. Under software control, following shared acPU (task) tasks, these events are treated and paid. Interrupts in our model are treated as events that are attached to real-time executive or tasks, favoring in this way the priority of the tasks to which they are attached. The lowest must be a real-time executive type. Once entered into the register, the one cannot be interrupted (interrupts are disabled). As a result, the executive functions must be done, without interruption and delay. The interrupt attached to a task can interrupt only strictly lower priority tasks, which are into the running state.

The solution is faster (Fig. 3) but requires an additional hardware block (Fig. 4) whose complexity is given by the total interrupts of the processor.

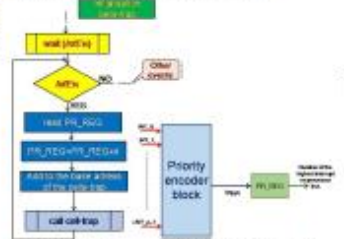


Fig. 3. Hardware solution

IMPLEMENTING THE ARCHITECTURE
 SPRA (Field Programmable Gate Array) device offers integrated elements of the complexity of the specific application oriented integrated circuits (ASIC - Application Specific Integrated Circuit), with the advantage of programmability or better said, of reprogrammability. FPGA devices allow the design of specialized hardware architectures with the advantage of flexibility programmable environment that is implemented. Currently, FPGA devices are equipped with equivalent capacity in logic gates that exceed the millions of logic gates at a low cost price. For this reason, the paper proposes an implemented hardware support for RTOS functionalities based on the FPGA systems.

The architecture will be study and implemented in VHDL, with FPGA Virtex5 or M6050 reference board (Fig. 5) produced by Xilinx.



Fig. 5. M6050 reference board

In the next period will implement in VHDL: context unit, data memory and instructions, hardware detection unit, forwarding unit, ALU, multiplexers, registers, PC, pipeline registers, etc (Fig. 6).

CONCLUSIONS

The presented paper defines new original functionalities for the mMPRA and mMPRA. It proposed an innovative solution for attaching the interrupts to the tasks (acPU). In this context, the interrupt binds the task's priority and behavior. Each interrupt's behavior is more predictable in the context of real-time application (a task cannot be interrupted only interrupts attached a more priority task). The proposed solution has some powerful and interesting features such as: does not need specialized interrupt controller, interrupts about the priority task (acPU), a task can attach again, several, or all the p-system interrupts, programmer sets the priority of the interrupt attached to the same task, interrupt attached to a task can interrupt a more priority task but cannot interrupt the execution of the task when is attached, or higher priority task, the interrupt may be attached to a single task, interrupt can be a task, all interrupts can be attached to a single task, interrupt doesn't need another acPU pipeline, it doesn't require saving and restoring the context, the interrupt can be tested, interrupt priorities can be dynamic (by reattaching to a task, or by changing the priority of the task to which it is attached). It proposed an innovative solution to provide interrupts attached to a task. Unlike long waiting solution descriptions, the proposed solution provides a unified response time for any interruption if the time is the only active interrupt. In addition, the proposed solution also provides fixed prioritized interrupts. We can say that the presented solution contains a unique interrupt management, and a hardware solution to attach the interrupts to the task of the hardware RTOS. In the future, we will explore ways to create the priority monitor block depending on the number of interrupts attached and possibly the direct hardware output to PC with the interrupt handler address.

CUPRINS

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Main author status:	PERFORM Project
Patent no.:	-
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Description of the invention:	The most effective interrupt handling is by hardware, which increases the speed of response to external events and reduces overload. Therefore, the hardware method is used in most of the RTOS. Analyzing traditional models for interrupts management found their inability to provide the temporal determinism required in real-time systems. The study refers to the architecture of a real-time scheduler implemented in hardware, which eliminates the override feature of the operating system and those determined by contexts' switching. First, the study proposes <i>Multi Pipeline Register Architecture</i> , which uses a unified space of priorities for tasks and interrupts, so there must be no specialized interrupts controller.
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