# Proceedings of
# 2014 18th International Conference on System Theory, Control and Computing (ICSTCC)

## (Joint conference SINTES 18, SACCS 14, SIMSIS 18)

October 17 - 19, 2014


**Editors:**
**Mihaela Hanako Matcovschi**
**Lavinia Ferariu**
**Florin Leon**


**Technical Co-sponsor:**

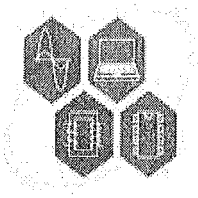
IEEE CSS

Institute of Electrical and Electronics Engineers - Control Systems Society

**Co-organizers:**

*Gheorghe Asachi* Technical University of Iasi
Faculty of Automatic Control and Computer Engineering

University of Craiova
Faculty of Automation, Computers and Electronics
Automatic Control Research Centre



*Dunarea de Jos* University of Galati
Faculty of Automatic Control, Computers,
Electrical and Electronics Engineering

**Copyright and Reprint Permission:** Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923. For reprint or republication permission, email to IEEE Copyrights Manager at pubs-permissions@ieee.org.
All rights reserved. **Copyright ©2014 by IEEE.**

**ISBN 978-1-4799-4602-0**

# A review of HDL-based system for real-time image processing used in tumors screening

Iuliana Chiuchisan, Oana Geman
Department of Computer Science, Electronics and Automation
Faculty of Electrical Engineering and Computer Science
"Stefan cel Mare" University of Suceava
Suceava, Romania
iulia@eed.usv.ro, geman@eed.usv.ro

***Abstract*—The use of hardware description languages to provide digital image processing results is a recent technique that offers a direct connection to reconfigurable hardware implementation. This paper presents a real time system for digital image processing using Verilog hardware description language that can be followed by immediate hardware implementation possibility. The image enhancement algorithms included in the described system were applied to an ultrasound image. The paper focuses on image enhancement methods such as contrast and brightness transformation, inverting and pseudo-coloring images, described and simulated using Verilog hardware description language. With our study we intend to contribute to the diagnoses of invasive and non-invasive methods in pre-operator stage, using modern VLSI technologies with applications in medical imaging.**

***Keywords*—*borderline tumors, medical imaging, real-time processing, VLSI technologies, hardware description languages, FPGA***

## I. INTRODUCTION

Potentially malignant ovarian tumors are rare entities with an excellent prognosis, which depends by the tumor stage of diagnoses. Ovarian pathology is currently among the largest gynecology complex problems - particular through ovarian tumors [1].

Ovarian cancer has a evolution that often starts insidiously, without specific symptoms and diagnosis occurrs during a routine exam. Although it was tried associating precursor lesions, results were not conclusive.

Worldwide, the incidence of ovarian cancer varies from continent to continent, the highest values being found in the Americas and the lowest in Japan and Africa. Global distribution of the incidence of ovarian cancer has no very great variety in spite of countless studies proving major variances. Data collected by the National Cancer Institute (USA) on the global distribution of the races in the incidence of ovarian cancer indicate that the white race is the most affected [3].

Malignant ovarian tumors are located at the position IV to the frequency of cancer in women, representing 15% of all female cancers. Generally in Romania ovarian cancer is diagnosed in advanced stages (III and IV) due to its evolution and symptoms absolutely uncharacteristic and due to the topography ovaries that is inaccessible clinical and in laboratory investigations.

In U.S.A., however, 75% of patients with malignant potential tumors are diagnosed in stage I. In this stage, survival over 5 years is 100%, but for patients diagnosed in advanced stages this percentage varies between 92% and 86% [4].

In Romania, ovarian cancer take 5$^{th}$ place in the category of cancers. Incidence is 4% of cancers among women, and the 5 year survival dependent on the stage of disease at diagnosis ranges between 50 - 55 % [5].

Tumors potentially malign (TPM) is a rare entity with an excellent prognosis depends greatly on stage of the tumor, and other factors. TPM is detected frequently in young women. Clinical examination and history is the starting point in elucidating the diagnosis but cannot alone confirm the presence of ovarian tumors [1]. The next step in the investigation of tumor of the ovary is the imaging [1]. Imaging diagnosis of ovarian cancer is essential using ultrasound or computed tomography [6].

With invasive ultrasound method can reveal ovarian tumors in early stages targeting the following parameters: size of the ovary, the size of the tumor mass, presence/absence of bilateral tumor morphology (content, wall, septa) and the predominance of solid/liquid/mixed [1], [7].

Among the methods for identifying malignant ovarian tumors risk include: ultrasound (non-invasive and invasive methods), ultrasound Doppler exploration and other modern imaging techniques. Ultrasonography is useful for diagnosis but the disease diagnostic cannot be based on ultrasound examination results alone. Ultrasound examination is conclusive only in the presence of other clinical factors or hormonal characteristic, as the use of tumor markers and other investigative techniques imaging [8].

## II. VLSI TECHNOLOGIES

Digital signal processing is applied in many domains such as mobile telephony, global positioning, radar and sonar detectors, biomedical imaging and many others.

ISBN 978-1-4799-4602-0 ©2014 IEEE

The digital signal processing has been the domain of the microprocessor [9]. For describing the behavior of the system the microprocessor executes a sequence of instructions. The advantage is that it does not require any modification of the circuit, but it cannot supply the same power consumption and processing performance as a reconfigurable hardware. Also, in case of microprocessor, a considerable portion of the circuitry is used for storage and control [9]. The advantage of reconfigurable hardware (field programmable gate array - FPGA), is that the hardware can be changed based on the computational needs and allows the acceleration to be achieved by a processor [9], [10].

The FPGA have become a complex platform that involves multiple hardware and software components. The FPGAs offer the ability to develop the most adequate circuit architecture for digital image processing systems. This reconfigurable hardware have the memory and power requirements in a similar way to systems on chip (SoC) [9].

The FPGA can be viewed as virtual hardware which can be dynamically reconfigured, can allow changes to the design between operation cycles and can implement functionality over the capacity available on the FPGA device [9]. The reconfigurable hardware can be reprogrammed or reconfigured by combining the parallel nature of combinational logic with the flexibility of software [10], [11]. The modern FPGA is a good choice for embedded real-time imaging systems because they offers sufficient resources in order to allow the systems to be implemented on a single FPGA.

The reconfigurable hardware is directly configured using Hardware Description Languages (HDL). For programming and reconfiguration of FPGAs we can use one of the two languages: Verilog HDL and Very High Speed Integrated Circuits Hardware Description Language (VHDL).

In the field of image processing the techniques that are usually used are expressed in the form of algorithms for processing, resulting the possibility of hardware implementation for image processing techniques using a modeling language such as Verilog HDL. High flexibility provided by hardware description languages allows the designers to logically describe much easier the system functionality, to simulate and evaluate the processing performances using appropriate development and test environments.

## III. HDL-BASED SYSTEM FOR REAL-TIME IMAGE PROCESSING

A real-time imaging system is the system that captures images, analyses them in order to obtain some data, and then uses that processed data to control some activity [11].

Given the importance of real-time image processing in medical activity and the significance of their implementations on hardware to achieve higher performance, this paper presents a novel hardware architecture of a real-time configurable system for image processing using image processing techniques, implemented in Verilog HDL and synthetized using reconfigurable hardware (FPGA).

The real-time image processing requirements demand a system ideally having characteristics such as high performance, flexibility, low-cost development [12], [13]. Recording to [14] "implementing image processing algorithms on reconfigurable hardware minimizes the cost, enable rapid prototyping of complex algorithms and simplifies debugging and verification".

The scope of our proposed real-time configurable system is for medical applications but can be used in any other area in which the speed of image processing in real time is vital. The real-time configurable system proposed in this paper provides a topical solution, being complementary, alongside the other classical processes for real-time applications.

In [15] and [16] was described the Verilog implementation of the real-time configurable system for image processing, using a series of basic image enhancement. A class of basic image processing operators that process an image so that the result is more suitable than the original image for a specific application were described in [17] and [18].

The system proposed in this paper is described in Verilog hardware description language at Register Transfer Level (RTL) and the images are digital processed by switching the order of filters and processing them to improve image in order to assist the medical specialists in diagnosis.

**Verilog code for output vector described using continuous assignment**

```
assign RGB_Out2[0] = PseudoColor_filter_order== 2?
RoutPseudoColor:  Contrast_filter_order  ==  2?
RoutContrast: Invert_filter_order== 2? RoutInvert:
RoutBrightness;

assign RGB_Out2[1] = PseudoColor_filter_order== 2?
GoutPseudoColor:  Contrast_filter_order  ==  2?
GoutContrast: Invert_filter_order== 2? GoutInvert:
GoutBrightness;

assign RGB_Out2[2] = PseudoColor_filter_order== 2?
BoutPseudoColorare:  Contrast_filter_order  ==  2?
BoutContrast: Invert_filter_order== 2? BoutInvert:
BoutBrightness;
```

The basic image processing operators, that for our system represent the filters, are described and used as internal components in the presented real-time configurable system for image processing. This components are connected in a pipeline structure, with the possibility of amending the order of filters and the parameters of each filter features.

**Verilog code for filters order in the system**

```
input [7:0] Filter_order;
assign PseudoColor_order = Filter_order [1:0];
assign Contrast_order = Filter_order [3:2];
assign Invert_order = Filter_order [5:4];
assign Brightness_order = Filter_order [7:6];
```

The configurable system includes 4 filters in order to improve the ultrasound image by switching and processing them by a series of filters. Using a single control input the system achieves to inter-change filters "on-the-fly", meaning that the design is dynamically reconfigured.

In Fig. 1 is presented a general architecture of the real-time configurable system for digital image processing.

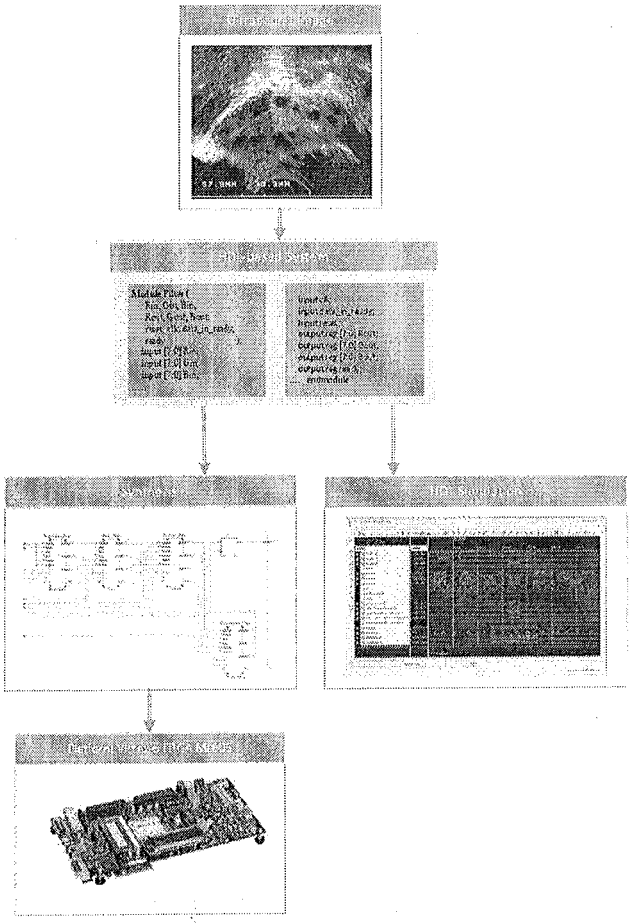


Fig. 1 Structure of real-time configurable system for digital image processing

Using HDL-based platform for image processing is a quite new approach extending the field of digital design to signal processing simulation. Since HDLs were designed to read binary files in ASCII format as inputs the basic idea of this research was to convert the input information in HDL readable data, pass those data through the virtually circuit described with Verilog, extract the binary results of the hardware simulation and convert them back into signal. All these actions are using the HDL development environment and its hardware simulation facilities [16].

## IV. Experimental Results

The results show the benefits that can be provided by the FPGA-based real-time configurable system implemented, since a considerable hardware resource reutilization is achieved.

The filters were described using Verilog hardware description language. The Verilog-based models were simulated using *ISIM Simulator* from *Xilinx ISE Design Suite*. In order to transform the initial image into a binary image that can be handled by the Verilog language we developed an application that converts images from Bitmap-format into a binary-format and stores them into an external file. The binary-file was applied as vector to the Verilog models. The output file was similarly converted and viewed using the same application, to show the original image and the results of the enhancement methods [12]. The class of image enhancement tested and simulated include contrast and brightness transformation, inverting and pseudo-coloring images.

Some of these filters have been encapsulated within the design tools and then applied to an ultrasound image in order to achieving efficient FPGA implementations in terms of area, speed and throughput rates and the parameters applied to filters are constant and were set by the user.

In the Fig. 2 and Fig. 3 (right panels) are illustrated the real-time processed ultrasound images.

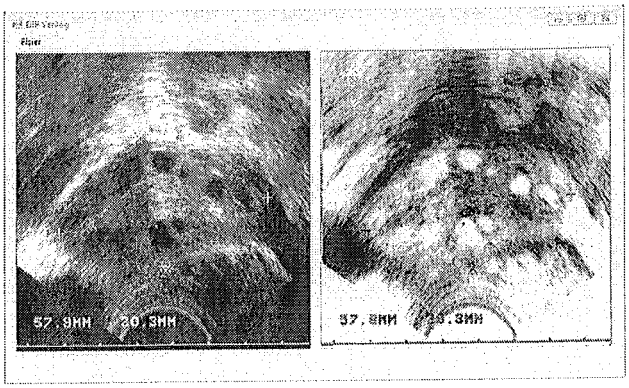


Fig. 2 Simulation results using ISIM Simulator

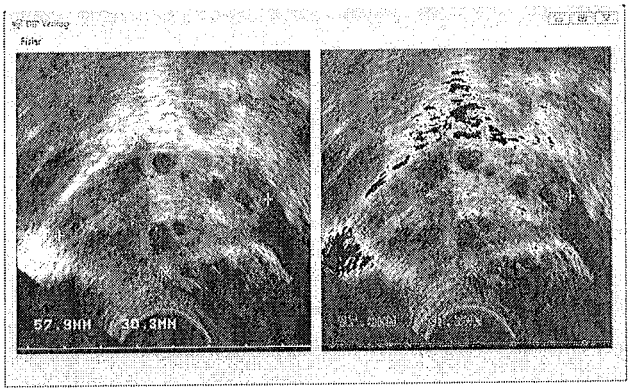


Fig. 3 Simulation results using ISIM Simulator

The class of digital processing algorithms described in our work is limited to basic algorithms but further research on complex image processing algorithms will be performed.

## V. Conclusions

The solution proposed in this paper offer a partial shift from imaging systems based on Digital Signal Processors (DSP) to image processing systems based on Reconfigurable Hardware (FPGA). The greater future potential of our proposed system lies in fact that it is not necessary to use an additional processor dedicated to image processing, which could slow down the flow: image acquisition → preprocessing the image → image use in order to establish a decision which can be human-type (in the case of a diagnosis based on medical images) or non-human (in the case of an industrial process).

There are some important advantages of our technique. The most important one is due to the fact that processing is always related with a hardware structure with immediate implementation availability and is not generated based on a mathematical only model. More, the use of digital design tools in signal processing simulations is offering a shorter way to the final implementation of processing circuit.

The technique described in this paper is part of a larger research oriented on the use of hardware description languages in signal processing simulations area. Other hardware processing simulations are to be studied as future work in order to evaluate and prove the advantage of this kind of approach. Extend the complex digital CAD tools into the signal processing field are offering not only a different developing solution but also a new larger implementation method which has to be considered together with the future digital technologies.

## ACKNOWLEDGMENT

This paper was supported by the project "*Sustainable performance in doctoral and post-doctoral research PERFORM*" - Contract no. POSDRU/159/1.5/S/ 138963, project co-funded from European Social Fund through Sectorial Operational Program Human Resources 2007-2013.

## REFERENCES

[1] K. Constantin, "Clinical-epidemiological, imagistic, histological and immunohistochemical study of ovarian mucinous tumors," PhD thesis, University of Medicine and Pharmacy Craiova, 2012.

[2] R.J. Kurman,I.M. Shih, "Pathogenesis of ovarian cancer: lessons from morphology and molecular biology and their clinical implications." Int J Gynecol Pathol. Apr; 27(2):151-60, 2008.

[3] T. Chen, L. Jansen, A. Gondos, K. Emrich, B. Holleczek, A. Katalinic, S. Luttmann, M. Meyer, H. Brenner, "Survival of ovarian cancer patients in Germany in the early 21st century: a period analysis by age, histology, laterality, and stage," Eur J Cancer Prev, 2012.

[4] Leading New Cancer Cases and Deaths – 2014 Estimates, http://www.cancer.org, 2014.

[5] Cancer Research UK, CancerStats Ovarian Cancer–UK, 2013.

[6] National Institutes of Health Consensus Development Conference Statement, Ovarian Cancer: Screening, treatment and follow-up, Gynecol Oncol, 55:S4-14, 2013.

[7] L.A.G Ries, J.L.Young, G.E. Keel, M.P. Eisner, Y.D. Lin, M.J. Horner, editors. SEER Program, NIH Pub. No. 07-6215. National Cancer Institute; Bethesda, MD: 2007. SEER Survival Monograph: Cancer Survival Among Adults: U.S. SEER Program, 1988–2001, Patient and Tumor Characteristics.

[8] D. Mureşan, F. Stamatian, "Modern techniques for ultrasound evaluation of ovarian tumors" (Tehnici moderne de evaluare ecografică a tumorilor ovariene), Obstetrica şi Ginecologia, LV(1): 13 – 57, 2007.

[9] R. Woods, J. McAllister, G. Lightbody, and Y. Yi, FPGA-based Implementation of Signal Processing Systems, John Wiley & Sons (UK) Publication, 2008.

[10] R. C. Gonzalez, R. E. Woods, Digital Image Processing, Prentice Hall, ISBN 0-13-094659-8, pp. 1-142, 2002.

[11] D. G. Bailey, Design for Embedded Image Processing on FPGAs, John Wiley & Sons (Asia), 2011.

[12] J. C. Russ, Image Processing Handbook, CRC Press, pp. 270-331, 2011

[13] W. Burger, M. J. Burge, "Principles of Digital Image Processing – Fundamental Techniques," Undergraduate Topics in Computer Science, DOI 10.1007/978-1-84800-191-6-4, 2009.

[14] S. Sowmya, R. Paily, "FPGA implementation of image enhancement algorithms", International Conference on Communications and Signal Processing (ICCSP), 2011, ISBN 978-1-4244-9798-0, pp 584 – 588, 2011.

[15] I. Chiuchisan and M. Cerlinca, „Implementation of Real-Time System for Medical Image Processing using Verilog Hardware Description Language," Proceedings of the 9th International Conference on Cellular and Molecular Biology, Biophysics and Bioengineering (BIO'13), ISSN: 1790-5125, ISBN: 978-960-474-326-1, pp.66-69, Chania, Creta, Greece, 2013.

[16] I. Chiuchisan, "A New FPGA-based Real-Time Configurable System for Medical Image Processing," Proceedings of IEEE International Conference on e-Health and Bioengineering – EHB 2013, ISBN 978-1-4799-2373-1, Iaşi, Romania, 2013.

[17] I. Chiuchisan, M. Cerlinca, A.D. Potorac and A. Graur, "Image Enhancement Methods Approach using Verilog Hardware Description Language," Proceedings of the 11th International Conference on Development and Application Systems, ISSN: 1844-5039, pp. 144-148, Suceava, Romania, 2012.

[18] I. Chiuchisan, "Implementation of Medical Image Processing Algorithm on Reconfigurable Hardware," Proceedings of IEEE International Conference on e-Health and Bioengineering – EHB 2013, ISBN 978-1-4799-2373-1, Iaşi, Romania, 2013.

[19] D. Venkateshwar Rao, S. Patil, N. A. Babu and V. Muthukumar, "Implementation and Evaluation of Image Processing Algorithms on Reconfigurable Architecture using C-based Hardware Descriptive Languages," International Journal of Theoretical and Applied Computer Sciences, vol. 1, no. 1, pp. 9–34, 2006.

[20] W. K. Pratt, Digital Image Procesing, John Wiley & Sons Publication, pp. 247-307, 2007.

[21] R. Maini, H. Aggarwal, "A Comprehensive Review of Image enhancement Techniques," Journal of Computing, vol. 2, issue 3, ISSN 2151-9617, pp. 269-300, 2010.

[22] P. S. Chikkali, K. Prabhushetty, "FPGA based Image Edge Detector and Segmentation," International Journal of Advanced Engineering Sciences and Technologies, vol. no. 9, issue no.2, pp 187-192, ISSN 2230-7818, 2011.