Improving Interrupt Handling in the nMPRA

Authors,
dr.eng. **Nicoleta Cristina GĂITAN**
Prof.dr.eng. **Vasile Gheorghita GĂITAN**
eng. **Elena-Eugenia (CIOBANU) MOISUC**

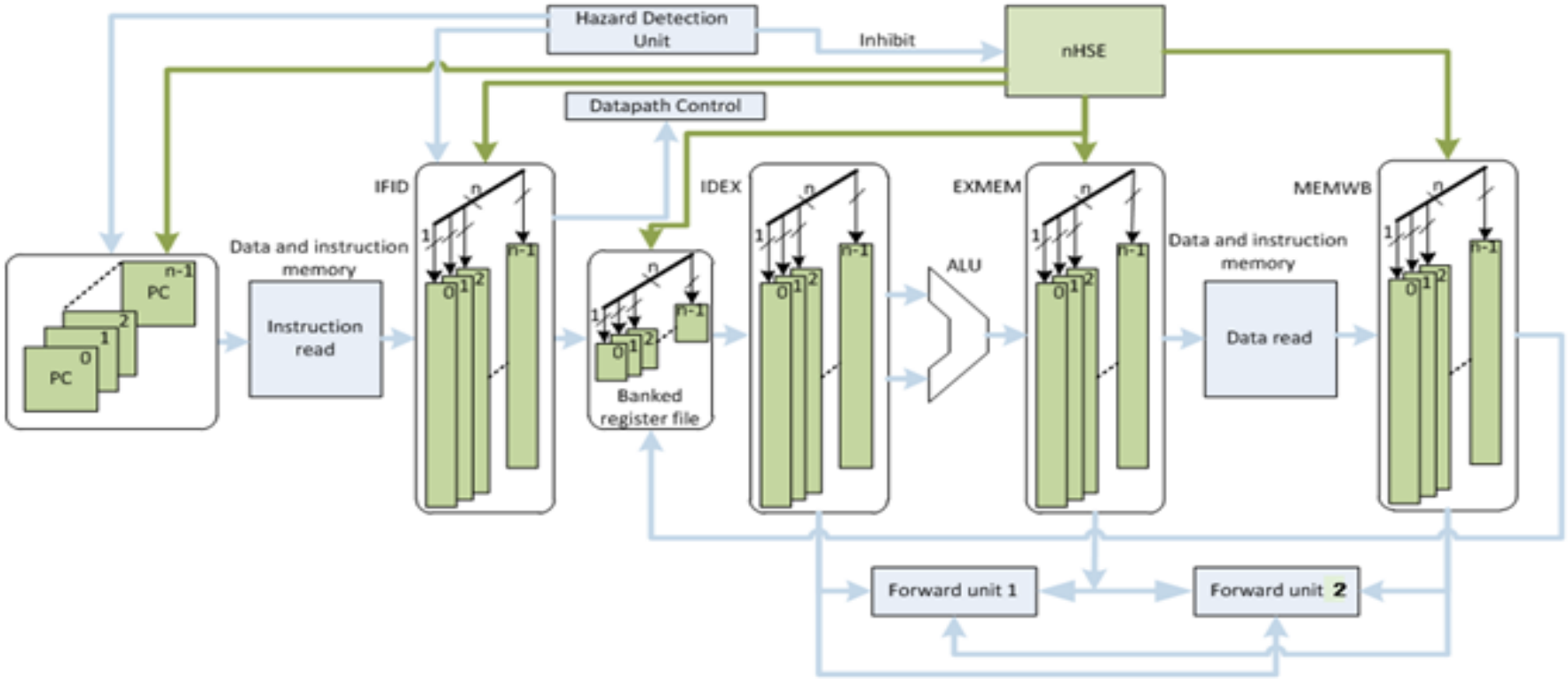
SUCEAVA 2014

Contents

1. Introduction (1)

- The research presented in this paper is based on the functional Multi Pipeline Register Architecture (MPRA) processor which provides a very low time for the context switching operations as a consequence of the architecture concepts. This processor is capable to perform automatic context switching and to start the new task in a range of 1 to 3 clock cycles.

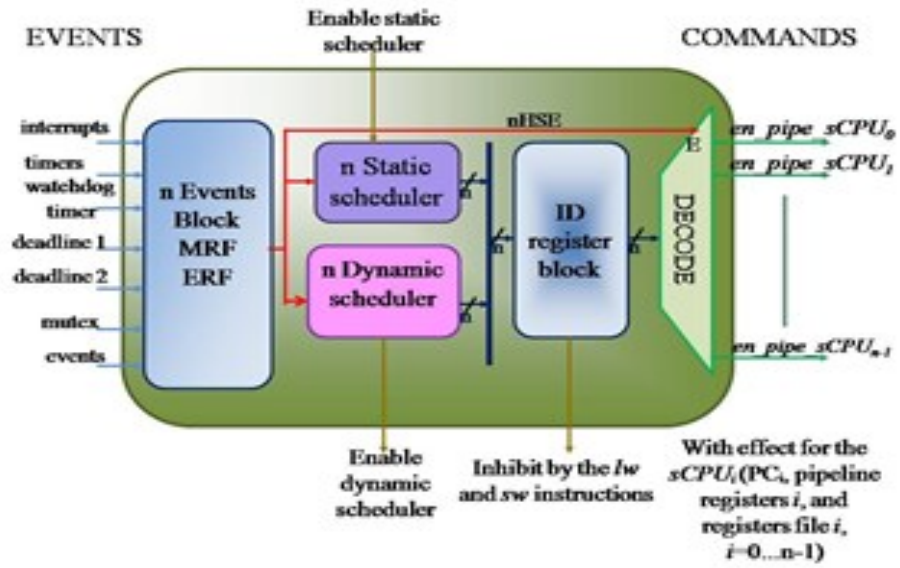
1. Introduction (2)



The context switching operations can be achieved in one processor cycle, and the response to an external event is delayed up to 1.5 processor cycles because each task has a set of pipeline.

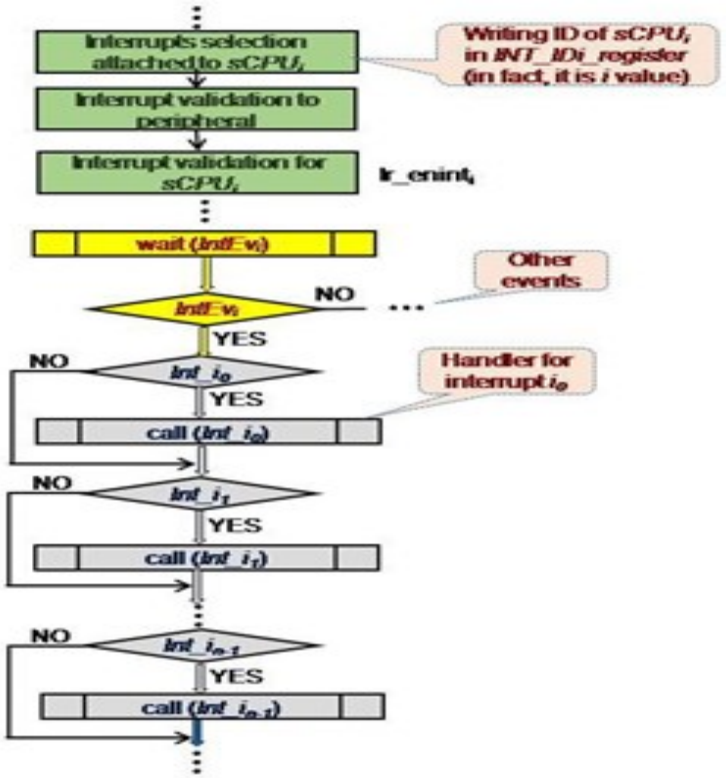
1. The nHSE architecture (1)

- The *nHSE* has input for events (interrupts, deadline, watchdog timers, timers, mutexes, message events, self-support event execution, as well enabling signals of static and dynamic schedulers and inhibiting the execution of load and store instructions) used to generate the $sCPU_i$ activation signals .



1. The nHSE architecture (3)

- The software solution it is simple (it does not require additional hardware modules) and versatile because the priorities of interrupts can be easily changed.



3. Conclusions (1)

- We improve the CPU architecture by an innovative solution for prioritization of the interrupts attached to the same task.

- Unlike loop testing solution, the proposed solution provides a uniform response time for any interrupt.

3. Conclusions (2)

- In the future, we will focus on the solution to create the priority encoder blocks depending on the number of attached interrupts and the possibility to upload direct to the CPU hardware the address of the interrupt handlers.

4. ACKNOWLEDGMENT

- The project “Sustainable performance in doctoral and post-doctoral research PERFORM–Contract no. POSDRU/159/1.5/S/138963”, project co-funded from European Social Fund through Sectorial Operational Program Human Resources 2007-2013.

5. References

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Thank
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Shukuria
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Biyan
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Juspaxar
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Proceedings of the

2014 International Conference on Development and Application Systems (DAS)

12th Edition, May 15-17, 2014, Suceava, Romania

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IEEE Catalog Number CFP1465Y-DVD

ISBN 978-1-4799-5092-8

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SECTION A - Systems, Process Control and Automations

SECTION B - Communications and Computer Networks

SECTION C - Electronics and Computer Aided Engineering

SECTION D - Software Engineering and Information Technologies

The 12th International Conference on Development and Application Systems DAS 2014

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Participant registration will take place in Building D, first Floor, on May 15 between 9:00 AM and 7:00 PM and on May 16, between 8:00 AM and 9:30 AM.

CONTACT INFORMATION

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Thursday - May 15, 2014

10:00 - 10:10 Opening Ceremony

Aula, Building E

Welcome message addressed by

Valentin POPA
Rector of Ştefan cel Mare University of Suceava

Adrian GRAUR
DAS 2014 Conference Chair

10:10 - 11:30 Plenary Session 1

Aula, Building E

Keynote Address

Haptics for Industry Applications

Kouhei OHNISHI
IEEE Fellow
Department of System Design Engineering
Keio University, JAPAN

Keynote Address

Eddy Current Nondestructive Evaluation – the Challenge of Accurate Modeling

Nathan IDA
IEEE Fellow
Department of Electrical and Computer Engineering
The University of Akron, USA

11:30 - 12:00 Coffee break

D101 - Building D

12:00 - 14:00 Technical Session 1

Location information on pages 8 and 11
Section A and Section B

14:00 - 15:00 Lunch break

University Restaurant

15:00 - 17:00 Technical Session 2

Location information on pages 13 and 16
Section C and Section D

17:00 - 17:30 Coffee break

D101 - Building D

17:30 - 18:50 Plenary Session 2

Aula, Building E

Keynote Address

Regulation and Command Systems in Power Converters with a Special Emphasis on the Resonant (and Wireless Energy) Converter

Stanimir VALTCHEV
IEEE Senior Member
Department of Electrical Engineering
Faculty of Science and Technology
Universidade Nova de Lisboa, PORTUGAL

Keynote Address

Petri nets Modeling and Distributed Embedded Controller Design

Luis GOMES
Faculty of Sciences and Technology
Universidade Nova de Lisboa, PORTUGAL

20:00 - 22:00 Cocktail Party

Bradet Restaurant

Friday - May 16, 2014

10:00 - 11:20 Plenary Session 3

Aula, Building E

Keynote Address

Are Unpaved Roads to Rome Better Than the Paved Ones?

Sorin D. COTOFANA
IEEE Senior Member
Department of Software and Computer Technology
Delft University of Technology, The NETHERLANDS

Keynote Address

Computer Integration of Spatially Distributed Systems

Dan Sorin NECSULESCU
Faculty of Engineering
University of Ottawa, CANADA

11:30 - 12:30 Poster Session

Aula, Building E

12:30 - 14:00 Lunch break

University Restaurant

14:00 - 15:00 H&S 2014 Public Presentations

Main Hall - Building E

15:00 - 16:00 Round table

Aula, Building E

16:00 - 17:30 H&S 2014 Award Ceremony

Main Hall - Building E

18:30 - 19:30 Departure to Sucevița

Parking lot of Building A

The transport from Suceava to Sucevița will be provided by the organizers. Accommodation for the 16.05 to 17.05 night, for all DAS 2014 participants, will be at Sofia Hotel, in Sucevița.

20:00 - 22:00 Official Dinner

Sofia Hotel / Sucevița

Saturday - May 17, 2014

09:00 - 10:00 Breakfast

Sofia Hotel / Sucevița

10:00 - 14:00 Monasteries Tour

Sucevița, Putna, Forest Equestrian Park Sucevița

14:00 - 17:00 Traditional Lunch

Sofia Hotel / Sucevița

17:15 - 18:30 Departure to Suceava

Thursday - May 15, 2014

Remus Răduleț Lecture Theatre, Building D

Technical Session 1

Systems, Process Control and Automations

12:00 - 14:00 Section A

Session Co-Chairs

Kouhei OHNISHI
Department of System Design Engineering, Keio University, JAPAN
Cornel TURCU
Ştefan cel Mare University of Suceava, Romania
Vasile Gheorghiță GĂITAN
Ştefan cel Mare University of Suceava, Romania

Paper ID: 11
Embedded Networked Monitoring and Control for Renewable Energy Storage Systems
Grigore STAMATESCU, Iulia STAMATESCU, Nicoleta ARGHIRA, Ioana FAGARASAN, Sergiu Stelian ILIESCU
Department of Automatic Control and Industrial Informatics
Politehnica University of Bucharest

Paper ID: 12
PID-Controller Application in the System for Variable Technological Process
Simion BARANOV[1], Irina COJUHARI[2], Ion FIODOROV[2], Leonid GORCEAC[3]
[1] Scientific and Engineering Centre "Informinstrument", Chişinău, Republic of Moldova
[2] Technical University of Moldova, Chişinău, Republic of Moldova
[3] State University of Moldova, Chişinău, Republic of Moldova

Paper ID: 13
Improving Interrupt Handling in the nMPRA
Nicoleta Cristina GAITAN, Vasile Gheorghita GAITAN, Elena-Eugenia (CIOBANU) MOISUC
Ştefan cel Mare University of Suceava, Romania

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Fuzzy Decision Support System for Solar Tracking Optimization
Iulia STAMATESCU, Grigore STAMATESCU, Nicoleta ARGHIRA, Ioana FAGARASAN, Sergiu Stelian ILIESCU
Department of Automatic Control and Industrial Informatics
Politehnica University of Bucharest

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Dorel AIORDACHIOAIE
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Mohamed BARARA[1], Ahmed ABBOU[1], Mohamed AKHERRAZ[1], Abderrahim BENNASSAR[1], Silviu IONITA[2], Emilian LEFTER[2], Bogdan ENACHE[2]
[1] University Mohamed V Agdal, Rabat, Morocco
[2] Faculty of Electronics, University of Pitesti, Romania

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Mykola ILASHCHUK, Eugene SOPRONIUK
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Robotic Arm Control in 3D Space Using Stereo Distance Calculation

Roland SZABO[1, 2], Aurel GONTEAN[1]

[1] Applied Electronics Department, Politehnica University of Timişoara

[2] Continetal Automotive România SRL Timişoara, Romania

Thursday - May 15, 2014

Nicolae Boţan Lecture Theatre, Building D

Technical Session 1

Communications and Computer Networks

12:00 - 14:00 Section B

Session Co-Chairs

Lieven De STRYCKER
Catholic University College Ghent, Association KULeuven, Belgium
Nicolae Dumitru ALEXANDRU
Gheorghe Asachi Technical University of Iaşi, Romania
Alin Dan POTORAC
Ştefan cel Mare University of Suceava, Romania

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Steven De LAUSNAY[1], Lieven De STRYCKER[1], Jean-Pierre GOEMAERE[1], Nobby STEVENS[1], Bart NAUWELAERS[2]
[1] Faculty of Engineering Science, DraMCo Research Group, KU Leuven, Gent, Belgium
[2] Faculty of Engineering Science, TELEMIC, ESAT, KU Leuven, Leuven, Belgium

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Nicolae Dumitru ALEXANDRU[1], Alexandra Ligia BALAN[2]
[1] Gheorghe Asachi Technical University of Iaşi, Romania
[2] Ştefan cel Mare University of Suceava, Romania

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Alin-Mihai CAILEAN[1,2], Barthelemy CAGNEAU[2], Luc CHASSAGNE[2], Valentin POPA[1], Mihai DIMIAN[1]
[1] University of Versailles Saint-Quentin, Vélizy, France
[2] Ştefan cel Mare University of Suceava, Romania

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Vakulabharanam RAMAKRISHNA[1], Tipparti Anil KUMAR[2]
[1] Department of Electronics & Communication Engineering, JNTUH, Hyderabad, India
[2] Department of Electronics & Communication Engineering, SR Engineering College, Warangal, India

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Design of a multi-input-multiple-output visible light communication system for transport infrastructure to vehicle communication
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Electronics and Computer Aided Engineering

15:00 - 17:00 Section C

Session Co-Chairs

Nathan IDA
University of Akron, USA
Constantin FILOTE
Ştefan cel Mare University of Suceava, Romania
Eugen COCA
Ştefan cel Mare University of Suceava, Romania

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Jeroen WYFFELS[1], Jos De BRABANTER[1], Jean-Pierre GOEMAERE[1], Bart NAUWELAERS[1], Lieven De STRYCKER[1], Piet VERHOEVE[2], Pieter CROMBEZ[2]
[1] Department of Electrical Engineering, KU Leuven, Heverlee, Belgium
[2] Televic Healthcare, B-8870 Izegem, Belgium

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Anneleen Van NIEUWENHUYSE[1], Frederic TORREELE[1], Jean-Pierre GOEMAERE[1], Lieven De STRYCKER[1], Bart NAUWELAERS[2]
[1] Faculty of Engineering Technology, KU Leuven, Gent, Belgium
[2] Department of Electrical Engineering, KU Leuven, Gent, Belgium

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Daniel CHIRUTA[1,2,3], Christian CHONG[1], Pierre-Richard DAHOO[4], Yasser ALAYLI[1], Mihai DIMIAN[3], Jorge LINARES[2]
[1] LISV, Université de Versailles Saint Quentin en Yvelines, Vélizy-Villacoublay 78140, France
[2] GEMAC, Université de Versailles Saint Quentin en Yvelines, Versailles, 78000, France
[3] Ştefan cel Mare University of Suceava, Suceava, 720229, Romania
[4] Université Versailles St-Quentin; Sorbonne Universités, UPMC Univ. Paris 06; CNRS/INSU, LATMOS-IPSL, Guyancourt, 78280, France

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[1] Ştefan cel Mare University of Suceava, Romania
[2] Alexandru Ioan Cuza University, Iaşi, Romania
[3] Advanced Materials Research Institute, University of New Orleans, New Orleans, U.S.A.

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Valentin OLESCHUK, Vladimir ERMURATSKII, Vladimir BERZAN
Academy of Sciences of Moldova, Chişinău, Republica Moldova

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Septimiu MOTOASCA
Transilvania University of Braşov, Romania

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Cristian-Gyozo HABA[1] , Derek PAPPAS[2]
[1] Gheorghe Asachi Technical University of Iaşi, Romania
[2] Yoterra Inc., Palo Alto, CA, USA

Paper ID: 66

Harmonic Analysis of Power Quality Indices Based on DWT using Three-Phase Modern Converters

Viorel APETREI, Constantin FILOTE, Adrian GRAUR
Ştefan cel Mare University of Suceava, Romania

Thursday - May 15, 2014

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Technical Session 2

Software Engineering and Information Technologies

15:00 - 17:00 Section D

Session Co-Chairs

Hariton Nicolae COSTIN
University of Medicine and Pharmacy Iasi, Romania
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Cristina Elena TURCU
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Mihai BARBULESCU, Mihnea IONESCU, Andrei Alexandru ENESCU
Freescale Semiconductor, Bucharest, Romania

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Institute of Computer Science, Romanian Academy, Iasi, Romania

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Adrian CIOBANU, Ioan PAVALOI, Mihaela LUCA, Elena MUSCA
Institute of Computer Science, Romanian Academy, Iasi, Romania

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Stefania–Iuliana SOIMAN, Ionela RUSU, Stefan-Gheorghe PENTIUC
Ştefan cel Mare University of Suceava, Romania

Paper ID: 49
A Second Order-Cone Programming Relaxation for Facility Location Problem
Vasile MORARU[1], Sergiu ZAPOROJAN[1], Adrian GROZA[2]
[1] Technical University of Moldova, Chisinau, Republic of Moldova
[2] Technical University of Cluj-Napoca, Cluj-Napoca, Romania

Paper ID: 54
Organization of High-Performance Parallel-Hierarchical Computing Processes for Classification of Laser Beam Images
Andriy A. YAROVYY[1], Leonid I. TIMCHENKO[2], Nataliya I. KOKRIATSKAIA[2], Svitlana V. NAKONECHNA[2], Maksym S. MATEICHUK[1]
[1] Vinnytsia National Technical University, Vinnytsia, Ukraine
[2] State University for Transport Economy and Technologies, Kyiv, Ukraine

Paper ID: 56
From Classical Computing to Quantum Computing
Adina BARILA
Ştefan cel Mare University of Suceava, Romania

Paper ID: 57
Romanian2SPARQL: A Grammatical Framework approach for querying Linked Data in Romanian language
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Technical University of Cluj-Napoca, Cluj-Napoca, Romania

Paper ID: 60
Spectral Analysis of Fetal Heart Rate Variability Associated with Fetal Acidosis and Base Deficit Values
Cristian ROTARIU, Alexandru PASARICA, Hariton COSTIN, Dragos NEMESCU
Grigore T. Popa University of Medicine and Pharmacy, Faculty of Medical Bioengineering, Iaşi, Romania

Notes

Notes

Notes

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Check Status

Submission ID: 13

Title: Improving Interrupts Handling in a nMPRA

Status: Accept

Reviewer Comments:

Several typos and mistakes.
Page 1
Improving Interrupts Handling => Improving Interrupt Handling
implement hardware interrupts handlers => implement hardware interrupt handlers
traditional models for interrupts management => traditional models for interrupt management
This paper presents an interrupts handler => This paper presents an interrupt handler
interrupts, so there is not specialized interrupts controller => interrupts, so there is no specialized interrupts controller
One of the fundamental requirements of RTS (Real-Time Systems) hard => One of the fundamental requirements of RTS (Real-Time Systems) hardware
the context switching operations of the tasks requires => the context switching operations of the tasks require
The MPRA provides a dynamic mechanism for the interrupts' management. => The MPRA provides a dynamic mechanism for the interrupt management.
Because of this acceptation rule fixed, that it is does not change => Because this acceptation rule is fixed, that is it does not change
Based on these devices, hardware supports for RTOS primitives [6] that can be easily implemented. => Based on these devices, hardware supports for RTOS primitives [6] can be easily implemented.
including an interrupts management => including an interrupt management
because each task has a set of pipeline register => because each task has a set of pipeline registers

Page 3
Analyzing scheme of interrupts, it noticed => Analyzing the scheme of interrupts, it was noticed
Another solution involves additional hardware block as => Another solution involves an additional hardware block as

Page 4
At the occurrence time of the interrupt, priority encoder => At the occurrence time of the interrupt, the priority encoder

Page 5
interrupts assigned to low priority tasks. => interrupts assigned to low-priority tasks.
by interrupts assigned lower priority tasks. => by interrupts assigned to lower priority tasks.
Interrupts follow the same execution procedure as tasks so that => Interrupts follow the same execution procedure as tasks, so that

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Authors specify in Conclusion that the paper presents an improved CPU architecture compared to their previous publications [1], and [2]. But compared to reference [3] are there any novelties? Reference [3] is highly cited in this paper and besides two elementary Karnaugh diagrams it seems to be no other news. Authors should reject the Karnaugh diagrams from the text as this is not intended to be a scholar review paper about minimizing Boolean expressions.